University of Stellenbosch

Department of Electrical & Electronic Engineering

Shunt active power filtering algorithms for unbalanced, non-linear loads

Marthinus Gerhardus Faculin Gous

12712507

Thesis presented in partial fulfilment of the requirements for the degree of Masters of Science in Electronic Engineering at the University of Stellenbosch.

Study leader: Dr. H.J. Beukes

December 2003

Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and has not previously in its entirety or in part been submitted at any university for a degree.

Ek, die ondergetekende verklaar hiermee dat die werk gedoen in hierdie tesis my eie oorspronklike werk is wat nog nie voorheen gedeeltelik of volledig by enige universiteit vir 'n graad aangebied is nie.

Summary

This thesis presents the design and implementation of shunt active power filtering algorithms for unbalanced, non-linear loads.

A three-phase four-wire topology is developed in the dq0 space. Based on this development an accurate dynamic system model, taking into account the effect of the neutral inductor is developed.

The synchronous reference frame technique is expanded to enable the isolation of the zero sequence current component into its instantaneous active and reactive current components. Additionally a prediction method is proposed that will enable the proper prediction of the reference currents in a three-phase four-wire system.

Two categories of reference current signal tracking algorithms are investigated; namely the predictive current controller and the sliding mode current controller. A compensating technique is proposed to compensate for the effects that sampling and computational time delay have on the performance of the system. Additionally, an investigation is done into the effect that dead-time has on the performance of the system, and based on this investigation a dead-time compensating strategy is proposed.

Finally simulation and practical results are provided to validate the discussed theories.

Opsomming

Hierdie verhandeling ondersoek die ontwerp en implementering van parralel gekoppelde aktiewe filter algoritmes vir ongebalenseerde, nie-lineêre laste.

'n Drie-fase vier-draad topologie, asook 'n korrekte model van die dinamiese sisteem , wat die effek van die neutraal induktor insluit, is ontwikkel in die dq0 ruimte. Die sinchroon verwysing vlak tegniek is uitgebrei om die isolering van die nul sekwensie stroom in onderskeidelik die oombliklike aktiewe en reaktiewe stroom komponente te verdeel. Addisioneel is a vooruitskatting tegniek aanbeveel wat die beheerder in staat sal stel om voldoende die verwysing strome vooruit te skat in 'n drie-fase vier-draad stelsel.

Twee katagoriee van verwysing stroom volging algoritmes is ondersoek, naamlik die afskatting stroom beheerder en die gleiende modus stroom beheerder. 'n Effektiewe kompensasie tegniek is voorgestel om die effek van tydvertraging as gevolg van monstering en verwerking te elimineer. Addisioneel is die effek van dooie-tyd ondersoek en gebasseer op hierdie ondersoek is 'n effektiewe dooie-tyd kompensasie tegniek voorgestel.

Laastens is simulasies en praktiese resultate verskaf om die werking van die voorgestelde teorie te bevestig.

Acknowledgements

I would like to thank the following people who made this thesis possible:

Dr. Johan Beukes for his guidance throughout the thesis.

To the members of the power electronic group, especially, Jacques du Toit, Gary Moor and Aniel Le Roux, for their help with the implementation of the software and the inverter hardware.

The foundation for research and development (FRD), ESKOM TSI, and the University of Stellenbosch for their financial assistance.

I am eternally grateful to my parents for their support throughout my studies. Thank you.

Lastly I would like to express my heartfelt gratitude towards Nicolette van Zyl for her patience, understanding and support for the last four years of my studies.

Table of Contents

Declaration i

Summary ii

Opsomming iii

Acknowledgements iv

LIST OF FIGURES x

LIST OF TABLES xviii

Glossary xix

1. Introduction 1

1.1 Background 1

1.2 Power-quality standards 1

1.2.1 NRS 048 2

1.2.2 IEC 61000 3

1.2.3 CENELEC EN 50160 5

1.2.4 IEEE 519 5

1.2.5 Evaluation criteria 7

1.3 Compensation configurations 8

1.3.1 Passive filters 8

1.3.2 Active filters 9

1.3.2.1 Type of converter structure 9

1.3.2.2 Topologies employed to realise active harmonic compensation 10

1.4 Selection of harmonic filters for specific applications 11

1.5 Thesis structure 13

2. Modelling of converters 14

2.1 Introduction 14

2.2 Different power inverter configurations 14
2.2.1 Single-phase inverters 14
2.2.2 Three-phase three-wire inverters 15
2.2.3 Three-phase four-wire inverters 17
2.2.3.1 Three-dimensional space vector PWM 19
2.2.3.1.1 Modulation limiting methods 23
Inscribed ellipsoid limiting method 23
Boundary planes limiting method 24
2.2.3.1.2 Sequencing of switching vectors 25

2.3 Development of a dynamic system model for a three-phase four-wire system 27
2.3.1 Representing the inverter output voltages in terms of the inverter leg voltages in the dqo output space 27
2.3.2 The dynamic model of the three-phase four-wire topology 29

2.4 Summary 34

3. Reference signal-generating algorithms 35

3.1 Introduction 35

3.2 Generalised instantaneous reactive power theory 35

3.3 Extended synchronous reference frame technique 37

3.4 Prediction of the reference current 40

3.5 Comparison between the generalised instantaneous reactive power theory and synchronous reference frame technique 43
3.5.1 Voltage Unbalance 45
3.5.2 Voltage distortion 46
3.5.3 Load unbalance 47
3.5.4 Reactive power compensation 48

3.6 Summary 49

4. Reference signal-tracking algorithms 50

4.1 Introduction 50

4.2 Predictive current control 50
4.2.1 Simulation results 51

4.3 Variable structure control 53
4.3.1 Introduction 53
4.3.2 The switching function 55
4.3.3 Equivalent control 55
4.3.4 Reaching mode 56
4.3.4.1 Ideal saturating current controller 57
4.3.4.2 Tuning of reaching law approach 57
4.3.5 Simulation results 59
4.3.6 Summary 63

5. Practical considerations 65

5.1 Introduction 65

5.2 Time delay incorporated 65

5.3 Dead-time compensation techniques 71
5.3.1 Analysis of one phase arm 72
5.3.2 Four-leg inverter analysis on dead-time (mode 1) 74
5.3.3 Four-leg inverter analysis on dead-time (mode 2) 76
5.3.4 Dead-time compensation during a current direction change 79
5.3.5 Simulation results 80

5.4 Predictive current controller simulations using the proposed current controller algorithms 81

5.5 Sliding mode current controller simulations using the proposed current controller algorithms 84

5.6 Shunt active power filter simulations utilising the proposed controllers 91
5.6.1 Predictive current controller without the neutral inductor connected 91
5.6.2 Predictive current controller with the neutral inductor connected 92
5.6.3 Ideal saturating current controller without the neutral inductor connected 94
5.6.4 Ideal saturating current controller with the neutral inductor connected 96
5.6.5 Constant rate current controller without the neutral inductor connected 97
5.6.6 Constant rate current controller with the neutral inductor connected 99
5.6.7 Constant rate plus proportional current controller without the neutral inductor connected 101
5.6.8 Constant rate plus proportional current controller with the neutral inductor connected 102

5.7 Summary 104

6. Practical results of theory presented 108

6.1 Introduction 108

6.2 Space vector PWM 108

6.3 Current regulation 109

6.3.1 Predictive current control 110

6.3.2 Sliding mode controllers 116

6.4 Shunt Active power filtering 122

6.4.1 Predictive current controller – without neutral inductor 122

6.4.2 Predictive current controller – with neutral inductor 123

6.4.3 Ideal saturating current controller – without neutral inductor 125

6.4.4 Ideal saturating current controller – with neutral inductor 127

6.4.5 Constant rate current controller – without neutral inductor 128

6.4.6 Constant rate current controller – with neutral inductor 130

6.4.7 Constant rate plus proportional current controller – without neutral inductor 132

6.4.8 Constant rate plus proportional current controller – with neutral inductor 133

6.5 Summary 135

7. Conclusions and recommendations 139

7.1 Power-circuit configuration selection and modelling 139

7.2 Reference signal generating algorithms 139

7.3 Detailed design process for the current controllers 139

7.4 Practical implications 139

7.5 Practical results of theory presented 140

7.6 Recommendations and future work 141

7.7 Summary 141

References 142

Standards, Journal and Conference Papers 142

Books 145

Appendix - Modelling and control of converters 146

A-1 Explanation of orthonormality in 3x3 transformation 147

A-2 Legend to explain numbering of sectors (not to scale) 148

A-3 List of inverse matrices for the different sectors 149

A-4 Flowchart explaining process for determining the correct tetrahedron 152

A-5 The optimum switching sequence for the different sectors 153

A-6 Duty cycles for the different phase arms when in a specific sector 154

Appendix B Proofs 159

B-1 Illustrating the orthogonal and parallel component of a vector onto another vector 160

Appendix C Simulation and practical setup 161

C-1 Simulation and practical configuration 162

C-2 Simulation and practical configuration for shunt active power filter 163

C-3 Practical setup for testing the three-dimensional space vector PWM 164

Appendix D Source code 165

Code segment that transforms the line voltages and currents into the dq0 space 166

Three-dimensional space vector PWM code segment 166

Code segment that is doing the basic calculations 180

Code segment that generate the reference voltages 183

Code segment that compensate for dead-time effects 186

LIST OF FIGURES

Figure 1-1 (a) Shunt and (b) series passive filters 8
Figure 1-2 (a) CSI-type and (b) VSI-type inverter 9
Figure 1-3 Series active filter 10
Figure 1-4 Shunt active filter 10
Figure 1-5 Series-shunt active filter 11
Figure 1-6 Hybrid active filter 11
Figure 2-1 Single-phase half-bridge inverter 14
Figure 2-2 Single-phase full-bridge inverter 15
Figure 2-3 A three-phase 3-leg inverter 15
Figure 2-4 Normalised leg space projection onto the normalized output space 16
Figure 2-5 A three-phase four-leg inverter 17
Figure 2-6 A four-dimensional cuboid's projection onto the three-dimensional output space 18
Figure 2-7 The projection of the 16 switching vectors in the dq0 output space 19
Figure 2-8 A graphical representation of the sectors 20
Figure 2-9 Top view of Figure 2-8 21
Figure 2-10 Optimum switching sequence for sector 1 22
Figure 2-11 Limiting ellipsoid inside the polyhedron [15] 23
Figure 2-12 Category 1 switching schemes (a) Rising-edge aligned, (b) Falling-edge aligned, (c) Symmetrically aligned, (d) Alternative sequencing scheme 25
Figure 2-13 Category 2 switching schemes (a) Rising-edge aligned, (b) Falling-edge aligned, (c) Symmetrically aligned, (d) Alternative sequencing scheme 26
Figure 2-14 The Dynamic model as proposed by [12] 29
Figure 2-15 Representation of the inductors connected between the load and the four-leg inverter 29
Figure 3-1 Voltage and current vector representation in rotating dq0 space 38
Figure 3-2 Voltage and current vector representation in rotating dq0 space (top view) 38
Figure 3-3 Voltage and current vector representation in rotating dq0 space 39
Figure 3-4 Explanation of time delay 40
Figure 3-5 The complete process for predicting the future value of the reference vector 43
Figure 3-6 Three-phase four-wire network used for simulation studies 44
Figure 3-7 Ideal condition waveforms (equivalent for both reference algorithms) (a) Phase A load current, (b) Phase A compensating current, (c) Phase A compensated source current, (d) Neutral current with (magenta trace) and without (blue trace) compensation 45
Figure 3-8 (a) Supply voltage unbalance, (b) Compensated source currents using GIRPT, (c) Compensated source currents using synchronous reference frame technique 46
Figure 3-9 Summary of the results under unbalanced supply voltage conditions 46
Figure 3-10 a) Phase A supply voltage distortion, (b) Compensated phase A source current using GIRPT, (c) Compensated phase A source current using Synchronous reference frame technique 47

Figure 3-11 Summary of the results when the supply voltage is distorted 47
Figure 3-12 3-13 a) Phase A load current, Phase B and C =0, (b) Compensated source currents using GIRPT, (c) Compensated source currents using synchronous reference frame technique 48
Figure 3-14 Summary of the results when there is a 100% load unbalance 48
Figure 3-15 Reactive power compensation (a) uncompensated phase A load current and supply voltage, (b) compensated phase A source current and supply voltage using GIRPT, (c) compensated phase A source current and supply voltage using the proposed extended synchronous reference frame technique 49
Figure 4-1 Predictive current control with neutral inductor not connected (a) 50 Hz sinusoidal, and (b) 50 Hz square waveforms 52
Figure 4-2 Predictive current control with neutral inductor connected (a) 50 Hz sinusoidal, and (b) 50 Hz square waveforms 52
Figure 4-3 Equivalent inductance values for an 800 µH inductor 53
Figure 4-4 Equivalent resistance values for an 800 µH inductor 53
Figure 4-5 Explanation of sliding mode control 54
Figure 4-6 Control scheme outline of the proposed sliding mode controller 54
Figure 4-7 Continuous-approach switching functions 56
Figure 4-8 Sliding mode controller – ideal saturating controller with neutral inductor not connected 59
Figure 4-9 Sliding mode controller – ideal saturating controller with neutral inductor connected 60
Figure 4-10 Sliding mode controller – Constant rate controller with neutral inductor not connected 61
Figure 4-11 Sliding mode controller – Constant rate controller with neutral inductor connected 61
Figure 4-12 Sliding mode controller – Constant rate + proportional controller with neutral inductor not connected 62
Figure 4-13 Sliding mode controller – Constant rate + proportional controller with neutral inductor connected 62
Figure 5-1 Predictive current controller without neutral inductor connected, using sinusoidal references, with no prediction implemented 67
Figure 5-2 Predictive current controller without neutral inductor connected, using square references, with no time delay compensation implemented. 67
Figure 5-3 Predictive current controller with neutral inductor connected, using sinusoidal references, with no time delay compensation implemented. 68
Figure 5-4 Predictive current controller with neutral inductor connected, using square references, with no time delay compensation implemented. 68
Figure 5-5 Explanation of the oscillations when the time delay compensation is not implemented 69
Figure 5-6 Predictive current controller without neutral inductor connected, using sinusoidal references, with time delay compensation implemented. 69
Figure 5-7 Predictive current controller without neutral inductor connected, using square references, with time delay compensation implemented. 70

Figure 5-8 Predictive current controller with neutral inductor connected, using sinusoidal references, with time delay compensation implemented. 70
Figure 5-9 Predictive current controller with neutral inductor connected, using square references, with time delay compensation implemented. 71
Figure 5-10 Three-phase 4-leg inverter used to aid in the discussion 72
Figure 5-11 One-leg of the three-phase four-leg inverter 72
Figure 5-12 Effect of dead-time on one-leg of inverter 73
Figure 5-13 Effect of dead-time on the phase-to-phase voltages when in mode 1 74
Figure 5-14 Effect of dead-time on the phase-to-phase voltages when in mode 2 77
Figure 5-15 Calculation of compensating times for mode 2 79
Figure 5-16 Illustrating the effect when reference current change direction 80
Figure 5-17 Predictive current controller with neutral conductor (a) no dead-time compensation (b) dead-time compensation using only the actual current directions (c) dead-time compensation using the reference current vector 81
Figure 5-18 Predictive current controller without neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented..... 82
Figure 5-19 Predictive current controller without neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented..... 82
Figure 5-20 Predictive current controller with neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented..... 83
Figure 5-21 Predictive current controller with neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented..... 83
Figure 5-22 Ideal saturation controller without the neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented..... 84
Figure 5-23 Ideal saturation controller without the neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented..... 85
Figure 5-24 Ideal saturation controller with the neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented..... 85
Figure 5-25 Ideal saturation controller with the neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented..... 86
Figure 5-26 Constant rate controller without the neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented..... 87
Figure 5-27 Constant rate controller without the neutral inductor connected, using square references, with time delay and dead-time compensation implemented. 87
Figure 5-28 Constant rate controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented. 88
Figure 5-29 Constant rate controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented. 88
Figure 5-30 Constant rate plus proportional controller without the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented. 89

Figure 5-31 Constant rate plus proportional controller without the neutral inductor connected, using square references, with time delay and dead-time compensation implemented. 89
Figure 5-32 Constant rate plus proportional controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented. 90
Figure 5-33 Constant rate plus proportional controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented. 90
Figure 5-34 Simulation results showing (a) load current, and (b) compensated source currents 91
Figure 5-35 Simulation results showing phase A (a) load current, (b) compensating current, and (c) compensated source current..... 91
Figure 5-36 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 92
Figure 5-37 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace) 92
Figure 5-38 Simulation results showing (a) load current, and (b) compensated source currents 93
Figure 5-39 Simulation results showing phase A (a) load current, (b) compensating current, and (c) compensated source current..... 93
Figure 5-40 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 93
Figure 5-41 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace) 94
Figure 5-42 Simulation results showing (a) load current, and (b) compensated source currents 94
Figure 5-43 Simulation results showing phase A (a) load current, (b) compensating current, and (c) compensated source current..... 95
Figure 5-44 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 95
Figure 5-45 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace) 95
Figure 5-46 Simulation results showing (a) load current, and (b) compensated source currents 96
Figure 5-47 Simulation results showing phase A (a) Load current, (b) compensating current, and (c) compensated source current..... 96
Figure 5-48 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 97
Figure 5-49 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace) 97
Figure 5-50 Simulation results showing (a) load current, and (b) compensated source currents 98
Figure 5-51 Simulation results showing phase A (a) Load current, (b) compensating current, and (c) compensated source current..... 98
Figure 5-52 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 98

Figure 5-53 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace) 99
Figure 5-54 Simulation results showing (a) load current, and (b) compensated source currents 99
Figure 5-55 Simulation results showing phase A (a) Load current, (b) compensating current, and (c) compensated source current 100
Figure 5-56 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 100
Figure 5-57 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace) 100
Figure 5-58 Simulation results showing (a) load current, and (b) compensated source currents 101
Figure 5-59 Simulation results showing Phase A (a) load current, (b) compensating current, and (c) compensated source current 101
Figure 5-60 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 102
Figure 5-61 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace) 102
Figure 5-62 Simulation results showing (a) load current, and (b) compensated source currents 103
Figure 5-63 Simulation results showing Phase A (a) load current, (b) compensating current, and (c) compensated source current 103
Figure 5-64 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 103
Figure 5-65 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace) 104
Figure 6-1 Space vector PWM modulating balanced voltages (a) currently implemented, (b) new three-dimensional space vector PWM 108
Figure 6-2 Space vector PWM modulating unbalanced voltages (a) currently implemented, (b) new three-dimensional space vector PWM 109
Figure 6-3 Predictive current controller without neutral inductor connected, using sinusoidal references, with no time delay compensation implemented. 110
Figure 6-4 Predictive current controller without neutral inductor connected, using square references, with no time delay compensation implemented. 110
Figure 6-5 Predictive current controller with neutral inductor connected, using sinusoidal references, with no time delay compensation implemented. 111
Figure 6-6 Predictive current controller with neutral inductor connected, using square references, with no time delay compensation implemented. 111
Figure 6-7 Predictive current controller without neutral inductor connected, using sinusoidal references, with time delay compensation implemented. 112
Figure 6-8 Predictive current controller without neutral inductor connected, using square references, with time delay compensation implemented. 112

Figure 6-9 Predictive current controller with neutral inductor connected, using sinusoidal references, with no time delay compensation implemented. 113
Figure 6-10 Predictive current controller with neutral inductor connected, using square references, with time delay compensation implemented. 113
Figure 6-11 Predictive current controller without neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented..... 114
Figure 6-12 Predictive current controller without neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented..... 114
Figure 6-13 Predictive current controller with neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented..... 115
Figure 6-14 Predictive current controller with neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented..... 115
Figure 6-15 Ideal saturation controller without the neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented..... 116
Figure 6-16 Ideal saturation controller without the neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented..... 116
Figure 6-17 Ideal saturation controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented. 117
Figure 6-18 Ideal saturation controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented. 117
Figure 6-19 Constant rate controller without the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented. 118
Figure 6-20 Constant rate controller without the neutral inductor connected, using square references, with time delay and dead-time compensation implemented. 118
Figure 6-21 Constant rate controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented. 119
Figure 6-22 Constant rate controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented. 119
Figure 6-23 Constant rate plus proportional controller without the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented. 120
Figure 6-24 Constant rate plus proportional controller without the neutral inductor connected, using square references, with time delay and dead-time compensation implemented. 120
Figure 6-25 Constant rate plus proportional controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented. 121
Figure 6-26 Constant rate plus proportional controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented. 121
Figure 6-27 Practical results showing (a) load current, and (b) compensated source currents 122
Figure 6-28 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current..... 122

Figure 6-29 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 123
Figure 6-30 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current 123
Figure 6-31 Practical results showing (a) load current, and (b) compensated source currents 124
Figure 6-32 Practical results showing phase A (a) Load current, (b) compensating current, and (c) compensated source current 124
Figure 6-33 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 124
Figure 6-34 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current 125
Figure 6-35 Practical results showing (a) load current, and (b) compensated source currents 125
Figure 6-36 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current 126
Figure 6-37 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 126
Figure 6-38 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current 126
Figure 6-39 Practical results showing (a) load current, and (b) compensated source currents 127
Figure 6-40 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current 127
Figure 6-41 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 128
Figure 6-42 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current 128
Figure 6-43 Practical results showing (a) load current, and (b) compensated source currents 129
Figure 6-44 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current 129
Figure 6-45 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 129
Figure 6-46 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current 130
Figure 6-47 Practical results showing (a) load current, and (b) compensated source currents 130
Figure 6-48 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current 131
Figure 6-49 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 131
Figure 6-50 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current 131
Figure 6-51 Practical results showing (a) load current, and (b) compensated source currents 132

Figure 6-52 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current 132
Figure 6-53 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 133
Figure 6-54 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current 133
Figure 6-55 Practical results showing (a) load current, and (b) compensated source currents 134
Figure 6-56 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current 134
Figure 6-57 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current 134
Figure 6-58 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current 135
Figure 7-1 Flowchart explaining process for determining the correct tetrahedron 152

LIST OF TABLES

Table 1 NRS 048 Maximum harmonic voltage levels 2
Table 2 NRS 048-2 voltage regulation limits 2
Table 3 Compatibility levels for individual harmonic voltages in low voltage networks 3
Table 4 IEC 61000-3-2 classes 3
Table 5 Stage 2 current emission values for single-phase, interphase and unbalanced three-phase equipment [38] 4
Table 6 EN 50160 maximum harmonic voltage levels 5
Table 7 Harmonic current distortion limits (I_h) in % of I_L 6
Table 8 IEEE 519 voltage distortion limits at the PCC 6
Table 9 Selection of active filters for specific application considerations [3] 12
Table 10 The 16 possible switching vectors 20
Table 11 Ideal saturating controller parameters 60
Table 12 Constant rate controller parameters 61
Table 13 Constant rate + proportional controller parameters 63
Table 14 Three combinations in mode 1 75
Table 15 Compensating times for the three discussed combinations in mode 1 76
Table 16 Actual average phase-to-phase voltages for mode 2 78
Table 17 Summary of the rms current error values 105
Table 18 Summary of the TDD values for the different current controllers 106
Table 19 Summary of the unbalance values for the different current controllers 107
Table 20 Summary of the rms current error values 136
Table 21 Summary of the TDD values for the different current controllers 137
Table 22 Summary of the unbalance values for the different current controllers 138
Table 23 Summary of the TDD values for the different current controllers 140
Table 24 List of inverse matrices for the different sectors 149
Table 25 The optimum switching sequence for the different sectors 153
Table 26 Duty cycles for the different phase arms when in a specific sector 154
Table 27 Parameters used to test the current controllers 162
Table 28 Parameters used to test the current controllers in a shunt active power filter 163
Table 29 Parameters used to test the current controllers 164

Glossary

EMI	Electromagnetic interference
PWM	Pulse width modulation
rms	Root mean square
THD	Total harmonic distortion
n,h	Order of harmonics
PWHD	Partial weighted harmonic distortion
S_{sc}	Short circuit power
$U_{nominal}$	Nominal system voltage
Z	Source impedance
PCC	Point of common coupling
S_{equ}	Rated apparent power of equipment
I_{equ}	Rated rms current
U_p	Rated voltage
I_{sc}	Maximum short-circuit current applied at PCC
I_L	Maximum demand load current
TDD	Total demand distortion
V_{pcc}	Voltage at PCC
V_h	Magnitude of individual harmonic components
V_n	Nominal system rms voltage
V_{zero}	Zero sequence voltage
V_{pos}	Positive sequence voltage
V_{neg}	Negative sequence component
I_h	Magnitude of individual harmonic current components
V_{rms}	rms voltage
CSI	Current source inverter
VSI	Voltage source inverter
V_{dc}	DC bus voltage
I_{dc}	DC bus current
i_c	Compensating current
i_L	Load current
i_s	Source current

V_{AF}	Series active filter voltage
kVA	kilo Volt-Ampere
Hz	Hertz
V_{An}, V_{Bn}, V_{Cn}	Three-leg inverter voltages with respect to load neutral
V_{Ag}, V_{Bg}, V_{Cg}	Three-leg inverter voltages with respect to inverter ground
DOF	Degrees of freedom
f	Either voltage or current component
f_0	Zero sequence component
$\mathbf{T}_{dqo}$	Transformation matrix that transform the three-leg inverter leg space to the output space
z	Placeholder component
$\mathbf{T}_{dqoz}$	Transformation matrix that transform the four-leg inverter leg space to the output space
S_a, S_b, S_c, S_n	State of leg in the inverter
$\mathbf{U}_{0..15}$	Switching vectors
$\mathbf{U}_{ref}$	Normalized reference vector
$\boldsymbol{\lambda}_1$, $\boldsymbol{\lambda}_2$, $\boldsymbol{\lambda}_3$	Scaled switching vectors
x_1, x_2, x_3, y_1, y_2, y_3, z_1, z_2, z_3	Components of the three switching vectors that comprise the boundary of the determined tetrahedron
d_1, d_2, d_3	Respective duty cycles
d_0	Zero state switching vector
D_A, D_B, D_C, D_N	Leg duty cycles for the four-leg inverter
$\mathbf{U}_{refl}$	Limited normalized reference vector
d_1', d_2', d_3'	Limited duty cycles
V_{AN}, V_{BN}, V_{CN}, V_N	Four-leg inverter leg voltages with respect to the point N
V_{Ag}, V_{Bg}, V_{Cg}, V_g	Four-leg inverter leg voltages with respect to ground (g)
V_d^*, V_q^*, V_0^*	dqo output space representation of the leg voltages with respect to ground (g)
$\mathbf{T}_{ln4}$	Matrix that relates the leg voltages with respect to ground (g) to the leg voltages with respect to N
V_d, V_q, V_0	Leg voltages with respect to n
r_l	Equivalent series resistance of the phase A, phase B and phase C filter inductor
r_N	Equivalent series resistance of the neutral inductor
L_A, L_B, L_C	Inductance of the phase A, phase B and phase C filter inductor
L_N	Inductance of the neutral inductor
i_C, i_B, i_A	Current through respective phase inductors

i_N	Current through neutral inductor/wire
u_d, u_q, u_0	Duty cycles in the dq0 output space
$\mathbf{V}_S$, $\mathbf{I}_L$	Vector representation of the voltage and current components in the dq0 space
GIRPT	Generalised instantaneous reactive power theory
P_L	Generalised instantaneous active power
$\mathbf{Q}_L$	Generalised instantaneous reactive power theory
Φ	Angle between $\mathbf{V}_S$ and $\mathbf{I}_L$
$\omega(t)$	Rate at which the rotating-dq0 axis rotates with regards to the stationary dq0 space
i_{drot}, i_{qrot}, i_{0rot}	Current components in the rotating dq0 space
$\mathbf{I}_P$	Parallel current component to $\mathbf{V}_S$
$\mathbf{I}_Q$	Orthogonal component to $\mathbf{V}_S$
DSP	Digital signal processor
T_s	Sampling period
$\Delta\Phi$	Time delay
$\mathbf{T}_f$	Period of the selected frequency component
a_n, b_n	Fourier coefficients
$\mathbf{u}_s$	Reaching control law
$\mathbf{u}_{eq}$	Equivalent control law
$\boldsymbol{\sigma}(\mathbf{x})$	Switching function
$\mathbf{x}^*$	Reference state vector
T_d	Dead-time
T_{on}	Turn-on time of switches
T_{off}	Turn-off time of switches
T_{pcom}	Compensating Time

1. Introduction

1.1 Background

In the modern world of advanced technology there is an increasing trend towards utilising more effective electrical and electronic components. These effective methods, such as power electronic devices in rectifiers, motor drives, power supplies, adjustable-speed drives in industrial systems, computer systems and electronic ballasts in commercial and consumer electronics, lead to major power-quality problems.

The majority of loads that use electrical energy as a power source have some degree of non-linearity and thus draw harmonic currents. These in turn cause a lot of power-quality problems, such as distorted voltages, voltage flickering, overheated transformers, high torque ripple in the generators, and severe EMI noise to communication and computer systems [7].

Power quality is even more degraded by the ever more popular use of non-linear, single-phase loads in three-phase electricity supply networks. This causes unbalance in the power supply system, which in turn may cause overheated neutral conductors and distorted sources.

All these factors typically force the utility to derate their components by as much as 80% [1]. There are various techniques currently available to compensate for the effects caused by the non-linear, unbalanced loads connected to the utility. The most common technique currently employed in industry for isolating three-phase load current harmonics from the supply is to connect a $\Delta - Y$ transformer between the three-leg inverter and the load. This, however, has some disadvantages [12]:

- $\Delta - Y$ transformers must be rated at the fundamental output frequency, which means that they are large, heavy and expensive, and impose additional losses to the system [12];
- Due to the harmonics caused by the loads and the PWM inverter, the $\Delta - Y$ transformer must be significantly overrated [12];
- Unbalanced or non-linear loads will cause the output voltage to distort due to the unavoidable leakage inductance of the transformer [12].

The aim of this thesis is to investigate a possible solution to compensate for the harmonics caused by non-linear unbalanced loads without making use of a $\Delta - Y$ transformer.

This chapter will discuss the standards, evaluation criteria and techniques which currently exist, or which are currently being developed in order to ensure a high degree of power quality.

1.2 Power-quality standards

In most applications in industry the economic incentives are not sufficient to bring about significant improvements in sustaining power quality; thus various standards were introduced to force the consumer and utilities to use lower harmonic power designs [8]. Four of these standards will be discussed in the subsequent sections.

1.2.1 NRS 048

The NRS 048 standard [9] was developed for the National Electricity Regulator of South Africa in order to set a standard for electricity distributors and customers. This standard, which is based on the IEC international standard and the CENELEC European standard, specifies minimum standards for various voltage quality parameters.

NRS states that the magnitude of each phase voltage harmonic must be obtained by taking the root mean square (rms) value of the supply voltage taken every 3 seconds for a period of 10 minutes. The highest 10-minute rms values recorded, which are not exceeded for 95% of the time in a 24-hour cycle, are the daily harmonic voltage magnitude. These measurements must be done for at least a continuous 7-day period.

The Total Harmonic Distortion (THD) of the supply voltage, which takes into consideration all the harmonics up to the order 40, must not exceed 8%. The maximum levels of individual voltage harmonics as specified by NRS 048-2 are specified in Table 1:

Table 1 – NRS 048 Maximum harmonic voltage levels

Odd harmonics non-multiples of 3		Odd harmonics multiples of 3		Even harmonics	
Order [h]	Harmonic Voltage [%]	Order [h]	Harmonic Voltage [%]	Order [h]	Harmonic Voltage [%]
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.3	6	0.5
13	3	21	0.2	8	0.5
17	2	>21	0.2	10	0.5
19	1.5			12	0.2
23	1.5			>12	0.2
25	1.5				
>25	0.2 + (1.3 x 25/h)				

The maximum deviation of the supply voltage from the standard voltages, as specified by NRS 048-2, is given in Table 2.

Table 2 – NRS 048-2 voltage regulation limits

Voltage level [V]	Compatibility Level [%]
< 500	± 10
≥ 500	± 5

Supply voltage unbalance is defined to be a maximum of 2% when predominantly three-phase systems are connected, and 3% when single-phase systems are connected. This value can be calculated by taking the weekly 10-minute rms value which is not exceeded 95% of the time.

1.2.2 IEC 61000

IEC is an international standard, but has only local applicability if adopted by a standards body, or a specific form of governance (regulator or law), or through customer specifications. On its own it has no weight; thus this standard only acts as a basis for local bodies to define their own standards or specifications [22]. A brief description of the IEC 61000 standards, which are relevant to the thesis, will now be given.

The IEC 61000-2-2 standard [36] provides guidelines for the permissible compatibility levels for low-frequency conducted disturbances and signalling in public low-voltage power supply systems. This standard divides the calculation of the harmonic voltage content into two categories: long-term effects, having a duration for longer than 10 minutes, and short-term effects. The maximum levels for individual voltage harmonics for long-term effects as specified by IEC 61000-2-2 are specified in Table 3.

Table 3 - Compatibility levels for individual harmonic voltages in low voltage networks

Odd harmonics non-multiples of 3		Odd harmonics multiples of 3		Even harmonics	
Order [h]	Harmonic Voltage [%]	Order [h]	Harmonic Voltage [%]	Order [h]	Harmonic Voltage [%]
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.4	6	0.5
13	3	21	0.3	8	0.5
$17 \le h \le 49$	$2.27 \times (17/h) - 0.27$	$21 \le h \le 45$	0.2	$10 \le h \le 50$	$0.25 \times (10/h) - 0.25$

When there are short-term effects present in the network, the individual harmonic components of the voltages are the values given in Table 3, multiplied with a factor k, where

$$k = 1.3 + \frac{0.7}{45} \times (h - 5) \tag{1-1}$$

The maximum allowable THD for long-term and short-term effects are 8% and 11% respectively.

The IEC 61000-3-2 [37] focuses on the permissible current rating of equipment drawing current less than 16 A. This standard divides equipment into 4 classes as shown in Table 4.

Table 4 - IEC 61000-3-2 classes

Class A	Balanced three-phase equipment and all other equipment, except that stated in one of the following classes
Class B	Portable tools, arc welding equipment which is not professional equipment
Class C	Lighting equipment, including dimming devices
Class D	Equipment having an input current with a special wave shape as defined in [37]

The IEC 61000-3-4 [38] focuses on the permissible current rating of equipment drawing currents more than 16 A. This standard provides three different assessment stages and it must be noted that if the

standard complies with one of these assessment stages a connection cannot be refused based on harmonic emissions.

Table 5 - Stage 2 current emission values for single-phase, interphase and unbalanced three-phase equipment [38]

Minimal R_{sce}	Admissible harmonic current distortion factors [%]		Admissible individual harmonic current I_n/I_1^* [%]					
	THD	PWHD	I_3	I_5	I_7	I_9	I_{11}	I_{13}
60	25	25	23	11	8	6	5	4
120	29	29	25	12	10	7	6	5
175	33	33	29	14	11	8	7	6
250	39	39	34	18	12	10	8	7
350	46	46	40	24	15	12	9	8
450	51	51	40	30	20	14	12	10
600	57	57	40	30	20	14	12	10
NOTE 1 – The relative value of even harmonics shall not exceed $16/n$ % NOTE 2 - Linear interpolation between successive R_{sce} values is permitted NOTE 3 – In the case of unbalanced three-phase equipment, these values apply to each phase								
* I_1 is the rated fundamental current								

In order to explain Table 5 four definitions are included as defined in IEC 61000-3-4:

- Partial weighted harmonic distortion (PWHD) is the ratio of the rms value of a selected group of higher-order harmonics (here beginning from the fourteenth harmonic), weighted with the harmonic order n to the rms value of the fundamental [38]:

$$PWHD = \sqrt{\sum_{n=14}^{40} \left(\frac{I_n}{I_1}\right)^2} \qquad (1\text{-}2)$$

- Short-circuit power (S_{sc}) is the value of the three-phase short-circuit power calculated from the nominal system voltage $U_{nominal}$ and the source impedance Z at the PCC [38]:

$$S_{sc} = \frac{U_{nominal}^2}{Z} \qquad (1\text{-}3)$$

- Rated apparent power (S_{equ}) of the equipment is the value calculated from the rated rms line current I_{equ} of the piece of equipment and the rated voltage U_p:

$$S_{equ} = 3U_p I_{equ-\max} \qquad (1\text{-}4)$$

where $I_{equ-\max}$ is the maximum value of the rms currents flowing in any one of the three phases

- The short circuit ratio (R_{sce}) can be defined as:

$$R_{sce} = \frac{S_{sc}}{S_{equ}} \text{ for all three-phase equipment} \quad (1\text{-}5)$$

Considering the discussed definitions the stage 2 current emission values for single-phase, interphase and unbalanced three-phase equipment are shown in Table 5.

1.2.3 CENELEC EN 50160

This standard was developed to "describe" the electrical product to ensure that claims could not be made against the product supplier, since the European legislation stipulates that if a product supplier does not define the usage of a product; any damages suffered by the client can be claimed from the product supplier [22].

The THD of the supply voltage, which takes into consideration all the harmonics up to the order 40, must not exceed 8%. The maximum levels of individual voltage harmonics as specified by EN 50160 are specified in Table 6.

Table 6 – EN 50160 maximum harmonic voltage levels

Odd harmonics non-multiples of 3		Odd harmonics multiples of 3		Even harmonics	
Order [h]	Harmonic Voltage [%]	Order [h]	Harmonic Voltage [%]	Order [h]	Harmonic Voltage [%]
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.5	6 - 24	0.5
13	3	21	0.5		
17	2				
19	1.5				
23	1.5				
25					

EN 50160 only defines voltage levels up to the order 25, since harmonics of an order higher than 25 are usually small and unpredictable due to resonance effects [23].

Supply voltage unbalance is defined to be a maximum of 2% when predominantly three-phase systems are connected, and 3% when single-phase systems are connected. This value can be calculated by taking the weekly 10-minute rms value which is not exceeded 95% of the time.

1.2.4 IEEE 519

IEEE 519-1992 [10] provides recommended limits for harmonic currents from individual customers and equipment at the point of common coupling (PCC). To ensure that the harmonic voltage levels in the overall power system will be acceptable, the standard recognises the divided responsibility between the customer and the utility [11].

The customer's responsibility lies in that he must limit the amount of current harmonics injected at the PCC. The current harmonic limits, which are expressed as a percentage of the customer's average

maximum demand load current, rather than as a percentage of the fundamental current, are given in Table 7.

Table 7 - Harmonic current distortion limits (I_h) in % of I_L

$V_n \leq 69kV$						
I_{sc}/I_L	$h<11$	$11 \leq h<17$	$17 \leq h<23$	$23 \leq h<35$	$h \geq 35$	TDD
<20	4	2	1.5	0.6	0.3	5
20-50	7	3.5	2.5	1	0.5	8
50-100	10	4.5	4	1.5	0.7	12
100-1000	12	5.5	5	2	1	15
>1000	15	7	6	2.5	1.4	20
$69kV < V_n \leq 161kV$						
<20*	2	1	0.75	0.3	0.15	2.5
20-50	3.5	1.75	1.25	0.5	0.25	4
50-100	5	2.25	2	1.25	0.35	6
100-1000	6	2.75	2.5	1	0.5	7.5
>1000	7.5	3.5	3	1.25	0.7	10
$V_n > 161kV$						
<50	2	1	0.75	0.3	0.15	2.5
≥ 50	3.5	1.75	1.25	0.5	0.25	4

I_{sc} is the maximum short-circuit current allowed at the PCC, and I_L is the maximum demand load current (rms value of the fundamental current component) at the PCC. I_L can be calculated as the average of the maximum monthly demands for the last 12 months, or if data are not available, it must be based on predicted load profiles. Table 7 only shows the individual harmonic limits for odd harmonics. The even harmonics limits are 25% of the limits shown.

Total Demand Distortion (*TDD*) is defined as shown:

$$TDD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_L} \times 100\% \qquad (1\text{-}6)$$

where I_h = magnitude of individual harmonic components (rms amps)

h = harmonic order

Table 8 - IEEE 519 voltage distortion limits at the PCC

Voltage at PCC	Individual voltage component distortion [%]	Maximum THD [%]
Vpcc < 69 kV	3	5
69 kV < Vpcc > 132 kV	1.5	2.5
Vpcc > 132 kV	1	1.5

The utilities' responsibility lies in that he must ensure that the voltage distortion limits at the PCC are not exceeded at the PCC even if all the customers connected at the PCC are within their current harmonic limits. The voltage distortion limits are shown in Table 8.

Total Harmonic Distortion (*THD*) is defined as shown:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_n} \times 100\% \tag{1-7}$$

where: V_h = magnitude of individual harmonic component (rms volts)

h = harmonic order

V_n = nominal system rms voltage

1.2.5 Evaluation criteria

The discussed standards will be used to evaluate the performance of the compensating device that will be developed.

In order to calculate the unbalance, the method of symmetrical components will be used [24]. This method enables the transformation of an unbalanced three-phase system into three balanced sequence networks as shown:

$$\begin{bmatrix} V_{zero} \\ V_{pos} \\ V_{neg} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{1-8}$$

where: $a = e^{j2\pi/3} = 1\angle 120^\circ$ and $a^2 = 1\angle 240^\circ$

In order to calculate the zero sequence and the negative sequence unbalance components, the following equations are used:

$$\text{Zero sequence unbalance} = \frac{\text{zero sequence component}}{\text{positive sequence component}} \times 100 \tag{1-9}$$

$$\text{Negative sequence unbalance} = \frac{\text{negative sequence component}}{\text{positive sequence component}} \times 100 \tag{1-10}$$

The performance of the current controllers will be evaluated by determining the rms value of the difference between the reference currents and the actual measured currents. The following equation will be used to calculate the rms value:

$$I_{rms} = \sqrt{\sum_{h=1}^{\infty} \left(\frac{I_h}{\sqrt{2}} \right)^2} \tag{1-11}$$

where I_h = magnitude of individual harmonic components

h = harmonic order

In order to evaluate the performance of the shunt active power filter the TDD will be determined as defined in Equation (1-6). I_L is taken as the maximum fundamental current component of the load current.

1.3 Compensation configurations

1.3.1 Passive filters

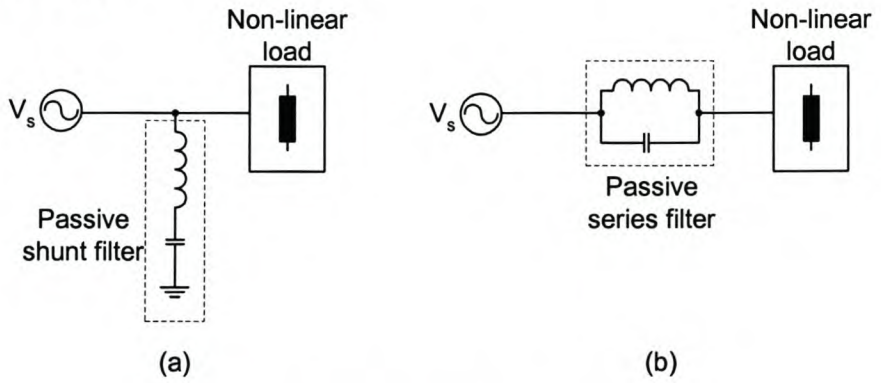


Figure 1-1 (a) Shunt and (b) series passive filters

Passive filters can be divided into two broad categories, namely shunt and series filters. Shunt passive filters provides a low impedance path for harmonic currents at their tuned frequency, while series passive filters offer a high impedance path at their tuned frequency. There are two reasons why shunt passive filters are more commonly installed [H1]:

- Shunt filters carry only a fraction of the load current, while series filters must carry the full load current, which implies that the series filter will generally be more bulky and more expensive;
- Shunt passive filters can be installed to supply reactive power at the fundamental frequency.

Passive filters, however, have several disadvantages:

- They can only compensate for preset frequencies; thus when the load or system parameters change, resonance can result;
- A passive filter cannot be used to compensate for a specific load's harmonics.

Because of these disadvantages, resonances can occur due to the interaction between passive filters and other loads, which may lead to unpredictable results [2]. This is the main reason that led to the development of dynamic and adjustable solutions to solve the power-quality problem, i.e. active filters [2], [3].

1.3.2 Active filters

Active filters can be classified into two broad categories:

- The type of converter structure employed;
- The topologies employed to realise active harmonic compensation.

1.3.2.1 Type of converter structure

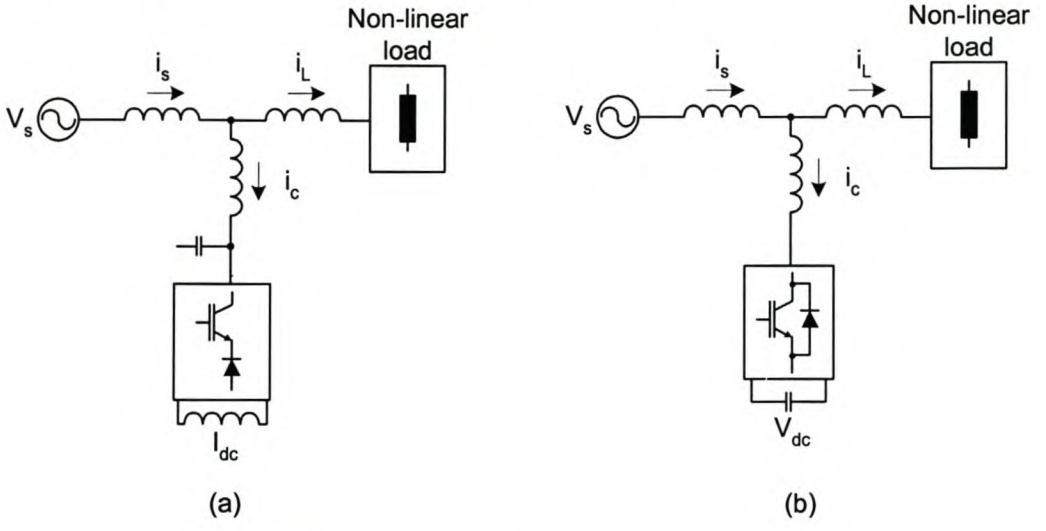


Figure 1-2 (a) CSI-type and (b) VSI-type inverter

The two types of converter structures being utilised in active filters are current source inverter (CSI) and voltage source inverter (VSI) structures.

Current source inverters use an inductor as an energy store. The control must be done in such a manner to ensure that there is always a current path for the current source and there must never be a short-circuit between two phases on the output side. Diodes are connected in series with the switches for reverse voltage blocking [3]. With a current source inverter only one of the switches in the top or bottom row is closed at any time in an n-phase system [4].

The voltage source inverter is the opposite of the current source inverter. It uses a capacitor to store its energy. The control must be done in such a manner to avoid the short-circuiting of the DC link capacitor and the sudden open circuit of any phases on the output side. Connecting reverse diodes in parallel across the switches can easily satisfy the second constraint. Thus in voltage source inverters each phase is switched either to the positive or negative DC rail [4].

Voltage source inverters are the preferred inverters due to their higher efficiency and their lower initial costs [5].

1.3.2.2 Topologies employed to realise active harmonic compensation

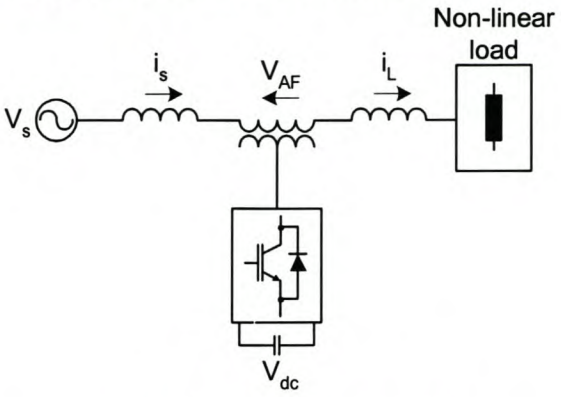


Figure 1-3 Series active filter

Series active filters are connected before the load in series with the mains by using a matching transformer. They are mainly used to eliminate voltage harmonics and to regulate and balance the terminal voltage at the point of common coupling. Electric utilities install them to compensate for voltage harmonics and to attenuate the harmonic propagation caused by resonances with line impedances and passive filters [3]. Series active filters and series passive filters do not compensate for current harmonics, but they act as a high impedance to current harmonics from the power source side [2].

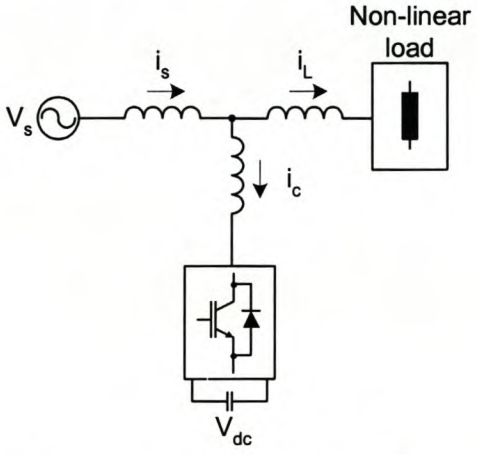


Figure 1-4 Shunt active filter

Shunt active filters work on the basis that non-linear loads inject harmonic currents into the grid. The active filter thus injects equal compensating currents, which are of opposite phase, into the grid to cancel these harmonic currents or reactive power components. Shunt active filters are used to compensate for current harmonics and reactive power (STATCON), and to balance unbalanced supply currents [3].

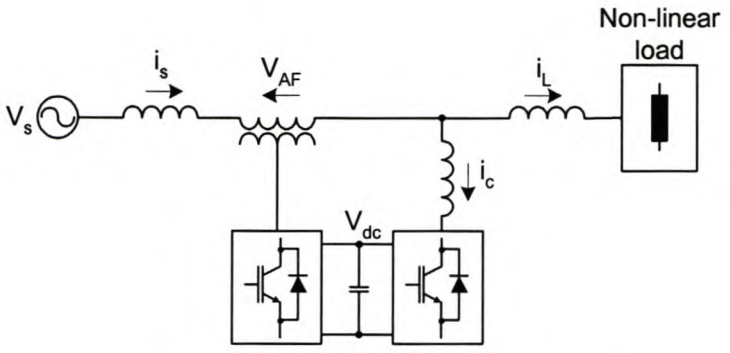


Figure 1-5 Series-shunt active filter

The series-shunt active filter configuration is deemed as the ideal active filter. It can eliminate voltage harmonics as well as current harmonics, but its major drawback is the high costs involved and the control complexity because of the large number of switches used [3].

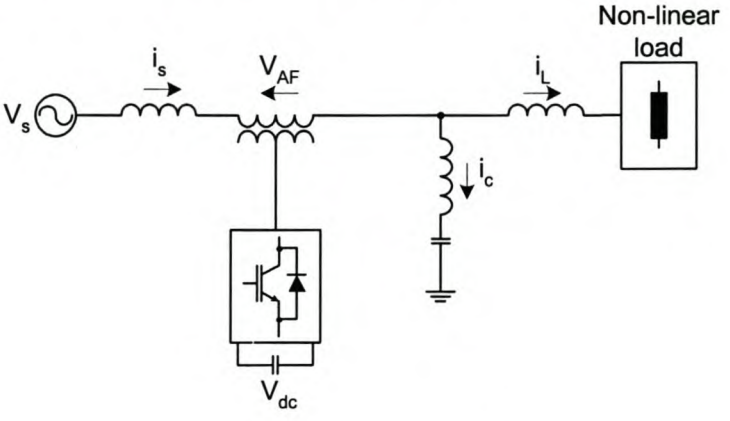


Figure 1-6 Hybrid active filter

Hybrid active filters consist of a combination of an active and a passive filter. The main reason for combining the passive filter with an active filter is to improve the performance of the passive filter and to reduce the initial costs. Currently the development of hybrid active filters is done mainly in a very unstructured fashion, building mainly on the existing tuned links [6]. Thus to aid the development of these filters the author of [6] formulated a systematic framework for identifying hybrid active filters based on the following criteria:

- Describing appropriate models for distorted loads;
- Determining the desirable attributes of the filter;
- Generating possible topologies in a systematic fashion.

1.4 Selection of harmonic filters for specific applications

Non-linear loads can be categorised into two broad categories, namely current harmonic sources and voltage harmonic sources.

Current harmonic source loads can be classified into this category when the current harmonics being injected by the load are not affected by the supply voltage waveform, while in voltage harmonic source loads the harmonic load currents being injected into the supply are highly dependent on the supply voltage waveform [13].

Thyristor converters are typical sources of harmonic currents and diode rectifiers with smoothing capacitors are typical sources of harmonic voltages.

[13] compares a list of 22 basic harmonic filter combinations and summarises them in the following categories: operating principles, type of non-linear loads that can be connected, circuit design and the control scheme employed, features and performance issues, as well as the VA rating and system cost.

Table 9 shows a general selection guideline for the type of configuration presented in the previous section [3]. The number of stars in Table 9 indicates the performance level.

Table 9 - Selection of active filters for specific application considerations [3]

Compensation for specific application	Active filters			
	Active series	Active shunt	Active series and passive shunt	Active series and active shunt
A. Current harmonics		**	***	*
B. Reactive power		***	**	*
C. Load balancing		*		
D. Neutral current		**	*	
E. Voltage harmonics	***		**	*
F. Voltage regulation	***	*	**	*
G. Voltage balancing	***		**	*
H. Voltage flicker	**	***		*
I. Voltage sags & Dips	***	*	**	*
(A + B)		***	**	*
(A + B + C)		**		*
(A + B + C + D)		*		
(E + F)	**			*
(E + F + H + I)	**			*
(A + E)			**	*
(A + B + E + F)			*	**
(F + G)	**		*	
(B + C)		*		
(B + C + D)		*		
(A + B + G)		**	*	
(A + C)		*		
(A + D + G)		*	**	

1.5 Thesis structure

The outline for this thesis is described briefly.

Chapter 2 discusses various power-circuit configurations which are utilised in active harmonic compensation. A three-phase four-wire topology will be developed in the dq0 space, as well as a true three-dimensional space vector PWM scheme. Additionally, the dynamic system model will be developed in the stationary dq0 space for the three-phase four-wire topology.

Chapter 3 discusses two reference signal-generating algorithms for shunt active power filters, as well as a prediction method that will enable the proper prediction of the reference currents in a three-phase four-wire system.

Chapter 4 discusses in detail the design process for the current controllers utilised to achieve proper reference current tracking. Two categories of current controllers will be investigated, namely predictive current controllers and sliding mode current controllers.

Chapter 5 discusses the practical implications when the current controllers are implemented practically. Practical issues that will be addressed are the effects that time delay and dead-time have on the reference current tracking performance. The performance of the discussed current controllers, as well as the shunt active power filter with the discussed current controllers implemented will be analysed in detail through simulations.

Chapter 6 will provide experimental results of the theory presented and finally Chapter 7 will conclude the thesis by giving a summary of the results and suggest opportunities for future research.

2. Modelling of converters

2.1 Introduction

In this chapter various power circuit configurations, which are utilised in active harmonic compensation, are discussed.

In order to explain the development of the three-phase, four-wire topology, a single-phase topology, and a three-phase three-wire topology will be discussed. Based on these two topologies a three-phase four-wire topology will be developed in the stationary dq0 space.

Additionally a true three-dimensional space vector PWM voltage control scheme will be developed in order to adequately address the problem of switching a three-phase four-leg inverter.

Further more, the dynamic system model in the stationary dq0 space for the three-phase four-wire topology as proposed by [12] will be proven incorrect and the correct dynamic model will be developed, which will take the effect of the neutral inductor into consideration.

2.2 Different power inverter configurations

2.2.1 Single-phase inverters

Single-phase inverters can be divided into half-bridge inverters as shown in Figure 2-1, and full-bridge inverters as shown in Figure 2-2.

The full-bridge inverters' maximum output voltage is twice that of the half bridge converter, and thus for the same power level the current through the switches in the full-bridge inverter is half the current flowing through the half-bridge inverters' switches.

Due to this fact full-bridge inverters are mainly used in high-power applications, and half-bridge inverters are generally used in low-power applications [H2].

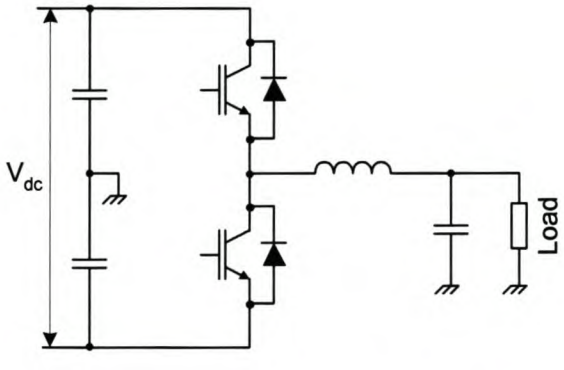


Figure 2-1 Single-phase half-bridge inverter

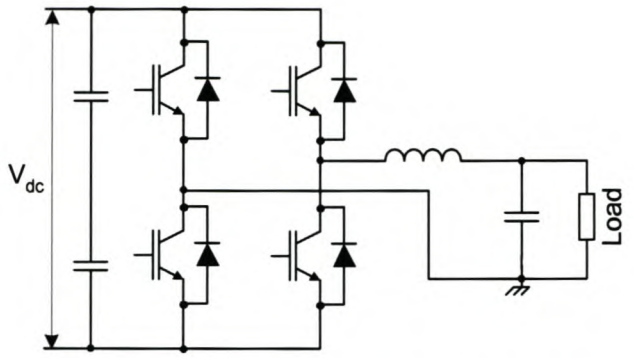


Figure 2-2 Single-phase full-bridge inverter

2.2.2 Three-phase three-wire inverters

For power levels above 10 kVA, it becomes advantageous to implement a three-phase inverter. The main advantage is that the instantaneous power in three-phase systems is constant, while in 50 Hz single-phase systems the power pulses at 100 Hz; thus all single-phase motors must be constructed to withstand an additional continual 100 Hz vibration [H3].

Figure 2-3 depicts a three-phase three-wire voltage source inverter with balanced LC output filters and loads.

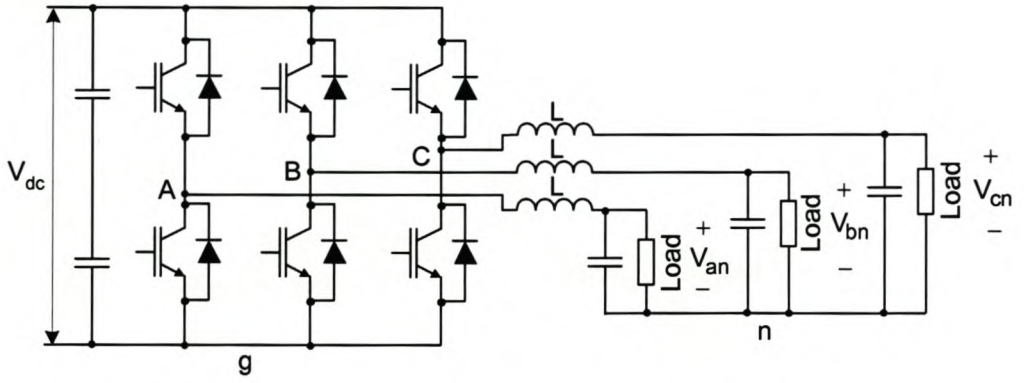


Figure 2-3 A three-phase 3-leg inverter

Three-leg (three-phase three-wire) inverters are developed for balanced three-phase loads. The phase voltages of the inverter with respect to the load neutral can be found in Figure 2-3:

$$V_{An} = V_{Ag} - V_{ng} \tag{2-1}$$

$$V_{Bn} = V_{Bg} - V_{ng} \tag{2-2}$$

$$V_{Cn} = V_{Cg} - V_{ng} \tag{2-3}$$

and by assuming a balanced filter and load, V_{ng} can be calculated as

$$V_{ng} = \frac{\left(V_{Ag} + V_{Bg} + V_{Cg}\right)}{3} \tag{2-4}$$

Equations (2-1) to (2-4) can now be represented in matrix form as shown in Equation (2-5).

$$\begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \end{bmatrix} \tag{2-5}$$

From this it can be seen that the maximum output voltage that a three-phase three-leg inverter can achieve is $2V_{dc}/3$.

The three-leg inverters' leg voltages $\left(V_{Ag},\ V_{Bg},\ V_{Cg}\right)$ can be represented as three orthogonal axes in the leg space. Since a three-leg inverter can only produce two independent voltages in the output space, the output space can be represented as a two-dimensional plane. Generalising an m-leg inverter can only be represented independently in a (m-1) dimensional output space [13]. The (m-1) dimensional output space can alternatively be called the (m-1) degrees of freedom (DOF) of the m-leg inverter. This representation of the three-leg inverter projection onto a 2 DOF dq plane orthogonal to the $[1\ \ 1\ \ 1]$ leg space vector is shown in Figure 2-4.

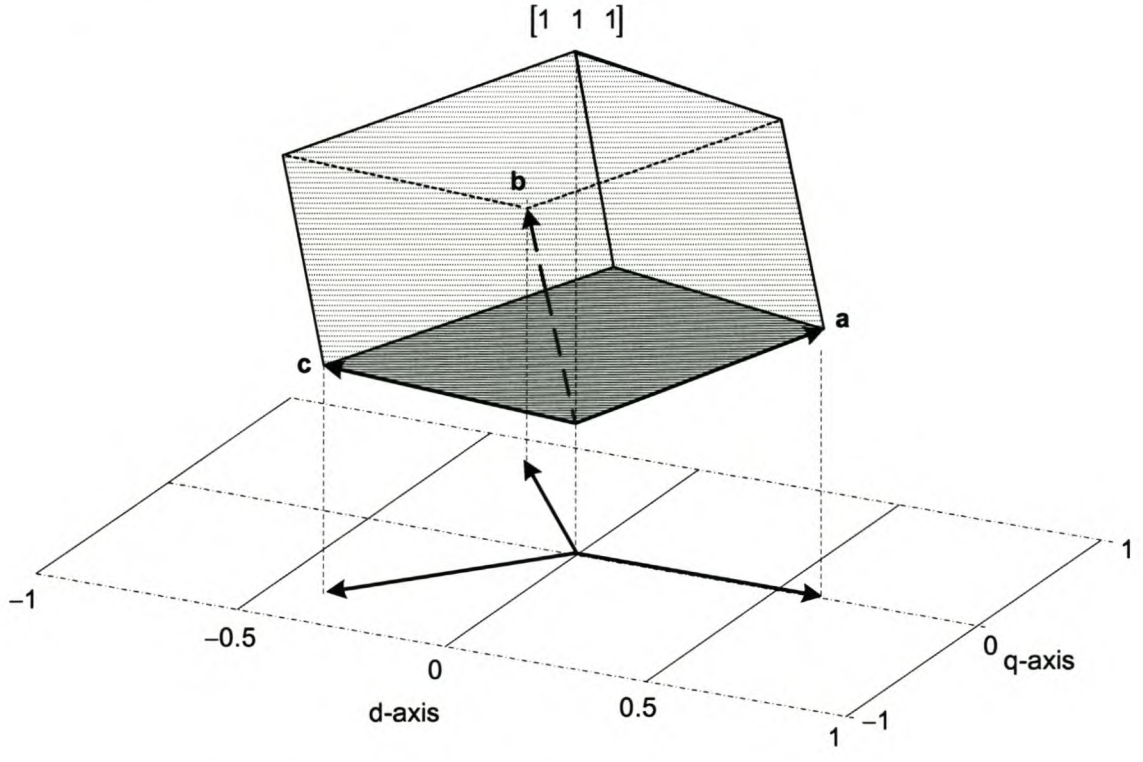


Figure 2-4 Normalised leg space projection onto the normalized output space

This transformation can be represented with the matrix:

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \bullet \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{2-6}$$

where f can be either a voltage or current component.

In order to transform backwards and forward (i.e. invertible matrix), f_0 or a "zero sequence" component is defined as a placeholder, thus a square and hence invertible matrix can be formed. To make the matrix orthonormal [H7], and thus simplifying computational effort, the matrix must be multiplied by $\sqrt{\frac{2}{3}}$. See Appendix A.

Finally the complete transformational matrix, $\mathbf{T}_{dqo}$, which transforms the leg space projection onto the output space, can be determined as shown:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \bullet \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{2-7}$$

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \mathbf{T}_{dqo} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{2-8}$$

2.2.3 Three-phase four-wire inverters

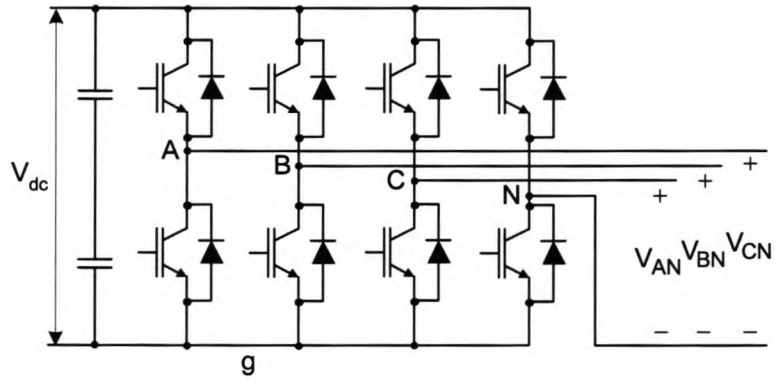


Figure 2-5 A three-phase four-leg inverter

Four-leg (three-phase four-wire) inverters are developed to power unbalanced, non-linear three-phase loads. A 4 x 4 decoupling transformation matrix, which is similar to the well-known 3 x 3 transformation matrix discussed in Section 2.2.2, was proposed by [12] to enable direct transformation from the four-leg inverter's leg modulation space to its corresponding 3 DOF output space.

The rest of this section will explain the concept of the 4×4 transformational matrix proposed by [12].

A four-dimensional cuboid, which represents the four-leg inverter, is projected onto the three-dimensional dqo output space as shown in Figure 2-6.

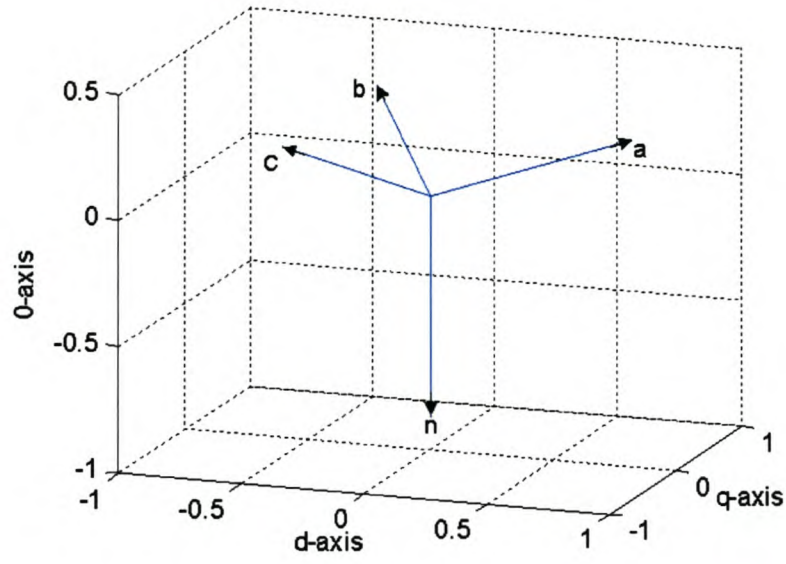


Figure 2-6- A four-dimensional cuboid's projection onto the three-dimensional output space

These projected vectors shown in Figure 2-6 must sum to zero:

$$a+b+c+n=0 \tag{2-9}$$

$$\begin{bmatrix} 1 \\ 0 \\ 1/2\sqrt{2} \end{bmatrix} + \begin{bmatrix} 1/2 \\ \sqrt{3}/2 \\ 1/2\sqrt{2} \end{bmatrix} + \begin{bmatrix} -1/2 \\ -\sqrt{3}/2 \\ 1/2\sqrt{2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ -3/2\sqrt{2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{2-10}$$

By combining these vectors to form a 4 x 4 transformation matrix, a placeholder "z" component must be added, as was done in Section 2.2.2, to ensure the backward and forward transformation being valid. To make the matrix orthogonal the z component values must be added as shown:

$$\begin{bmatrix} a & b & c & n \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix} \tag{2-11}$$

To make the matrix orthonormal, and thus simplifying computational effort, Equation (2-11) must be multiplied by a factor of $\sqrt{2/3}$. This produces the complete 4×4 transformation matrix, $\mathbf{T}_{dqoz}$, utilised in transforming the four-dimensional inverter leg space to the 3-DOF dq0 output space:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \\ f_z \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \\ f_n \end{bmatrix} = \mathbf{T}_{dqoz} \begin{bmatrix} f_a \\ f_b \\ f_c \\ f_n \end{bmatrix} \quad (2\text{-}12)$$

2.2.3.1 Three-dimensional space vector PWM

Three-dimensional space vector PWM is a voltage control scheme that adequately addresses the problem of switching a three-phase 4-leg inverter. In this section the 3-dimensional space vector PWM concept will be discussed in detail.

A 4-leg inverter has 16 possible switching states (vectors), assuming that the top and bottom "switches" of a phase arm work complimentary. The 16 possible switching states is shown in Table 10 and their projection in the dqo output space is shown in Figure 2-7.

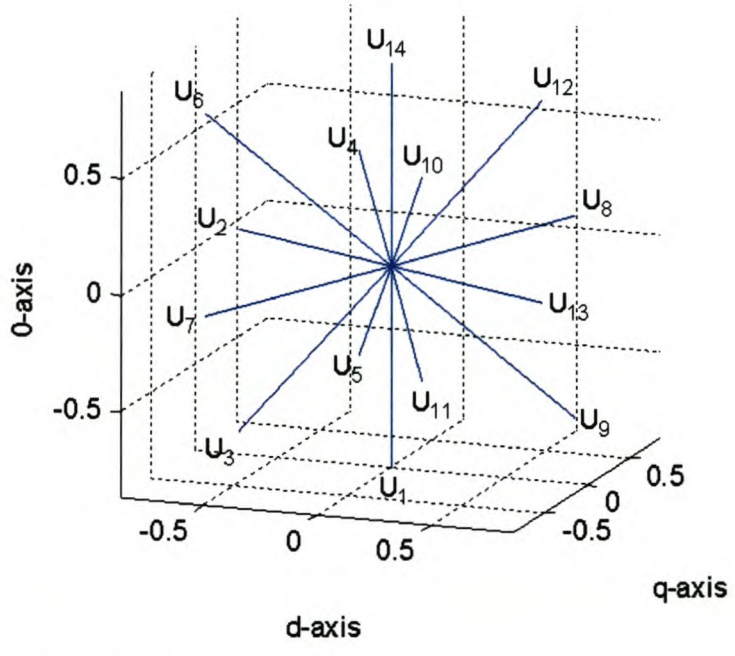


Figure 2-7 - The projection of the 16 switching vectors in the dq0 output space

The 16 possible switching vectors form 24 tetrahedrons (sectors) as shown in Figure 2-8. The tetrahedron in which a switching vector lies must be calculated, since when using a combination of the adjacent active switching vectors and the zero vectors, the circulating energy, current ripple and the harmonic content will be minimised [7]. In order to speed up the determination of the tetrahedron in which the reference vector lies, the algorithm can be divided into two steps.

Table 10 - The 16 possible switching vectors

Vector	*Sa*	*Sb*	*Sc*	*Sn*	*d*	*q*	*o*
U_0	0	0	0	0	0	0	0
U_1	0	0	0	1	0	0	-0.866
U_2	0	0	1	0	-0.4082	-0.7071	0.2887
U_3	0	0	1	1	-0.4082	-0.7071	-0.5774
U_4	0	1	0	0	-0.4082	0.7071	0.2887
U_5	0	1	0	1	-0.4082	0.7071	-0.5774
U_6	0	1	1	0	-0.8165	0	0.5774
U_7	0	1	1	1	-0.8165	0	-0.2887
U_8	1	0	0	0	0.8165	0	0.2887
U_9	1	0	0	1	0.8165	0	-0.5774
U_{10}	1	0	1	0	0.4082	-0.7071	0.5774
U_{11}	1	0	1	1	0.4082	-0.7071	-0.2887
U_{12}	1	1	0	0	0.4082	0.7071	0.5774
U_{13}	1	1	0	1	0.4082	0.7071	-0.2887
U_{14}	1	1	1	0	0	0	0.866
U_{15}	1	1	1	1	0	0	0

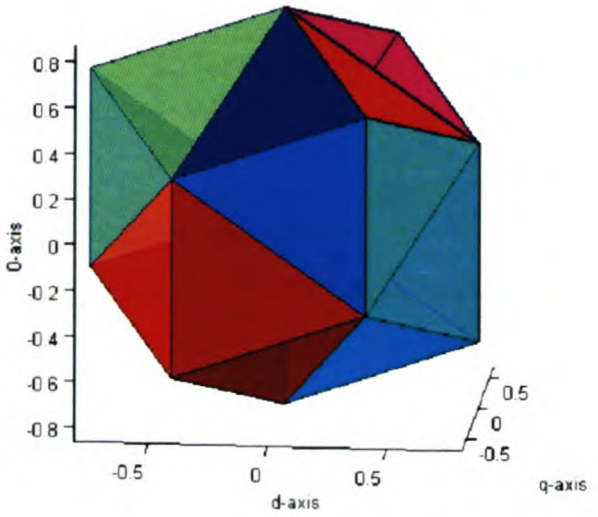


Figure 2-8 A graphical representation of the sectors

The first step is to determine the zone in which the reference vector lies using the top view, as shown in Figure 2-9, of the projection shown in Figure 2-8. The top view can be divided into six zones, which enables the same method to be used in determining the correct zone as is used to determine the sectors in a two-dimensional space vector PWM modulation technique.

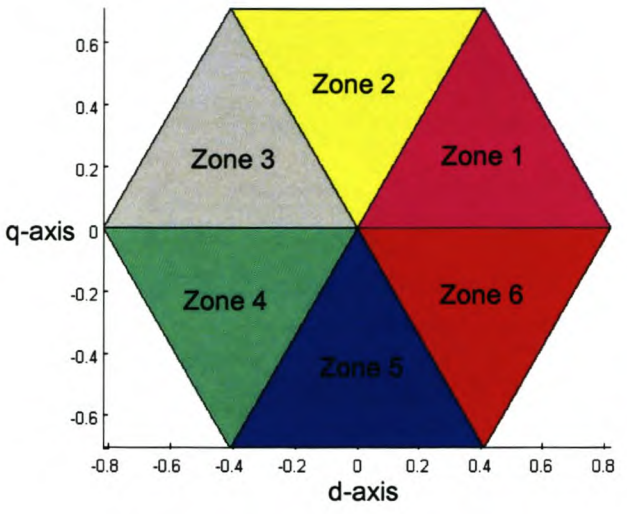


Figure 2-9 - Top view of Figure 2-8

Once the zone in which the reference vector lies is known, the second step is to determine in which tetrahedron the reference vector lies. There are 4 tetrahedrons in one zone and the correct tetrahedron can be calculated by determining the duty cycles for the active switching vectors. In order to calculate the duty cycles linear algebra is used. The rest of this section explains the process.

The known reference vector, $\mathbf{u}_{ref}$, can be defined as follows:

$$\mathbf{u}_{ref} = \frac{1}{V_{dc}}\left(V_d\hat{\mathbf{d}} + V_q\hat{\mathbf{q}} + V_o\hat{\mathbf{o}}\right) \tag{2-13}$$

The 3 vectors, $\boldsymbol{\lambda}_1$, $\boldsymbol{\lambda}_2$ and $\boldsymbol{\lambda}_3$, are scaled switching vectors that comprise the boundary of the determined tetrahedron is as follows:

$$\begin{aligned}\boldsymbol{\lambda}_1 &= d_1(x_1\hat{\mathbf{d}} + y_1\hat{\mathbf{q}} + z_1\hat{\mathbf{o}})\\ \boldsymbol{\lambda}_2 &= d_2(x_2\hat{\mathbf{d}} + y_2\hat{\mathbf{q}} + z_2\hat{\mathbf{o}})\\ \boldsymbol{\lambda}_3 &= d_3(x_3\hat{\mathbf{d}} + y_3\hat{\mathbf{q}} + z_3\hat{\mathbf{o}})\end{aligned} \tag{2-14}$$

where:

x_1, y_1, z_1, x_2, y_2, z_2, x_3, y_3 and z_3 are respectively the components, as given in Table 10, for the 3 switching vectors that comprise the boundary of the determined tetrahedron;

d_1, d_2 and d_3 are the respective duty cycles.

In order to determine the duty cycles the following equation must be satisfied:

$$\boldsymbol{\lambda}_1 + \boldsymbol{\lambda}_1 + \boldsymbol{\lambda}_1 = \mathbf{u}_{ref} \tag{2-15}$$

By rearranging Equations (2-13) to (2-15) in matrix form the duty cycles can be calculated as shown:

$$\mathbf{AB} = \mathbf{C}$$
$$\Rightarrow \mathbf{A}^{-1}\mathbf{AB} = \mathbf{A}^{-1}\mathbf{C} \qquad (2\text{-}16)$$
$$\Rightarrow \mathbf{B} = \mathbf{A}^{-1}\mathbf{C}$$

where

$$\mathbf{A} = \begin{bmatrix} x_1 & x_2 & x_3 \\ y_1 & y_2 & y_3 \\ z_1 & z_2 & z_3 \end{bmatrix} \qquad \mathbf{B} = \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} \qquad \mathbf{C} = \frac{1}{V_{dc}} \begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix}$$

Since matrix **A** consists of known constants, the inverse of matrix **A** can be calculated using Matlab®. The correct tetrahedron is known when all three calculated duty cycles are positive.

The complete set of inverse matrixes for the 24 tetrahedrons, as well as a chart showing the numbering of the 24 tetrahedrons, and a flow chart which summarises the three-dimensional space vector PWM process are given in Appendix A.

Once the duty cycles (d_1, d_2, d_3) have been calculated, they must be sequenced. The optimal switching sequence can be calculated by considering the minimum switching frequency, To obtain the minimum switching frequency for each inverter's leg, it is necessary that when a state change takes place only one inverter leg is switched [14]. Figure 2-10 shows the optimum switching sequence for sector 1, but a complete list of the optimum switching sequences for the 24 sectors is included in Appendix A.

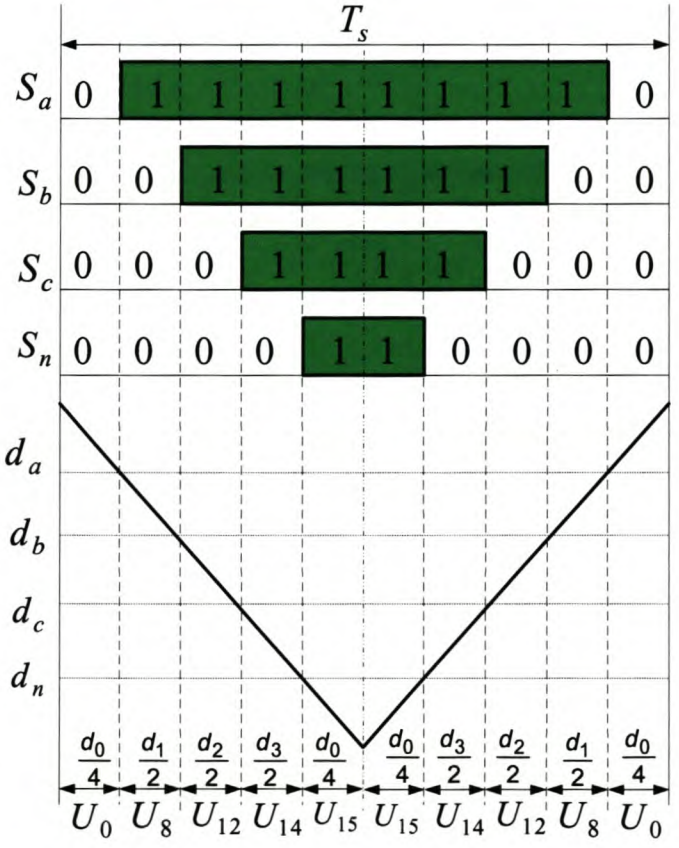


Figure 2-10 Optimum switching sequence for sector 1

When inside the linear region ($d_1 + d_2 + d_3 < 1$) the remaining "slack" must be taken up by the zero-state switching vectors to ensure that $d_1 + d_2 + d_3 + d_0 = 1$.

By keeping the optimum switching sequence in mind, the duty cycles for the different phase arms can be calculated as shown, provided that the reference vector lies in sector 1.

$$D_A = d_1 + d_2 + d_3 + \frac{d_0}{2} \quad (2\text{-}17)$$

$$D_B = d_2 + d_3 + \frac{d_0}{2} \quad (2\text{-}18)$$

$$D_C = d_3 + \frac{d_0}{2} \quad (2\text{-}19)$$

$$D_N = \frac{d_0}{2} \quad (2\text{-}20)$$

A complete list of the 24 sectors phase arm duty cycles is given in Appendix A.

2.2.3.1.1 Modulation limiting methods

The purpose of the limiting algorithms is to constrain the reference vector inside the polyhedron defined by the linear modulating region of the inverter. The linear modulation region refers to the fact that when the reference voltage vector is inside this region, there will be a linear relationship between the reference voltage and the output voltage. Two limiting algorithms will be discussed. The first algorithm is based on an inscribed ellipsoid on the boundary plane [15], and the second method is based on the polyhedron boundary planes.

Inscribed ellipsoid limiting method

The reference vector is limited to within the largest ellipsoid that can fit into the polyhedron as shown in Figure 2-11.

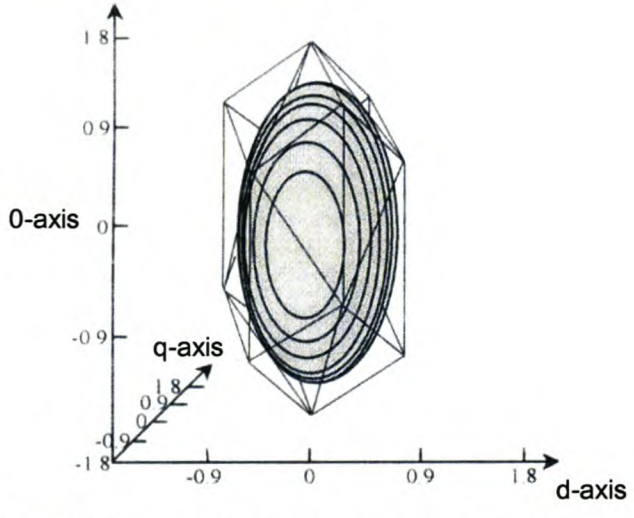


Figure 2-11 Limiting ellipsoid inside the polyhedron [15]

The largest polyhedron inscribed inside the polyhedron can be written as

$$\mathbf{u}_{ref}\mathbf{M}_{coef}\mathbf{u}_{ref}^{T} = 1 \tag{2-21}$$

$$\begin{bmatrix} V_d & V_q & V_0 \end{bmatrix}\mathbf{M}_{coef}\begin{bmatrix} V_d & V_q & V_0 \end{bmatrix}^{T} = 1 \tag{2-22}$$

where V_d, V_q, V_0 are the normalized reference voltages calculated, and $\mathbf{M}_{coef} = diag\begin{bmatrix} 2 & 2 & 0.5 \end{bmatrix}$ from [15]. It can be seen from Equation (2-21) that the reference vector, $\mathbf{u}_{ref}$, will be outside the ellipsoid if the following inequality is satisfied:

$$\sqrt{\mathbf{u}_{ref}^{T}\mathbf{M}_{coef}\mathbf{u}_{ref}} > 1 \tag{2-23}$$

Therefore, by using Equation (2-23), the reference vector $\mathbf{u}_{ref}$ can be limited to form a new vector, $\mathbf{u}_{refl}$, which will lie inside the ellipsoid:

$$\mathbf{u}_{refl} = \frac{\mathbf{u}_{ref}}{\sqrt{\mathbf{u}_{ref}^{T}\mathbf{M}_{coef}\mathbf{u}_{ref}}} \tag{2-24}$$

Boundary planes limiting method

This method limits the reference vector when it is outside the boundaries as defined by the 12-sided polyhedron shown in Figure 2-8.

The boundary of the 12-sided polyhedron can be defined as

$$d_1 + d_2 + d_3 = 1 \tag{2-25}$$

It can be seen from this equation that the reference vector, $\mathbf{u}_{ref}$, will be outside the boundary of the 12-sided polyhedron when the following inequality is satisfied:

$$d_1 + d_2 + d_3 > 1 \tag{2-26}$$

$\mathbf{u}_{ref}$ can be scaled by scaling d_1, d_2 and d_3 respectively in the following manner:

$$d_1' = \frac{d_1}{d_1 + d_2 + d_3} \tag{2-27}$$

$$d_2' = \frac{d_2}{d_1 + d_2 + d_3} \tag{2-28}$$

$$d_3' = \frac{d_3}{d_1 + d_2 + d_3} \tag{2-29}$$

To summarise: The inscribed ellipsoid method can generate sinusoidal output voltages when the reference vector is limited, but the main drawback is that it does not fully utilise the inverters' ability. The boundary planes method, however, limits the reference vector in such a manner that the limited vector allows a distorted voltage waveform. This can be interpreted in such a way as to say that the maximum rms value can be higher in the boundary planes method.

2.2.3.1.2 Sequencing of switching vectors

Once the duty cycles for the different phase arms are known, the next step is to sequence them. Sequencing of the switching vectors has no effect on the average vector within a switching period, but it can influence considerably the power losses and harmonic content [16]. In [7] the sequencing schemes are summarised in two broad categories. Category 1 uses both of the zero-switching vectors, U_0, U_{15}, while category 2 uses only one of the two zero-switching vectors.

Figure 2-12 illustrates for two consecutive switching periods the different switching schemes for category 1, when the reference vector lies in sector 1.

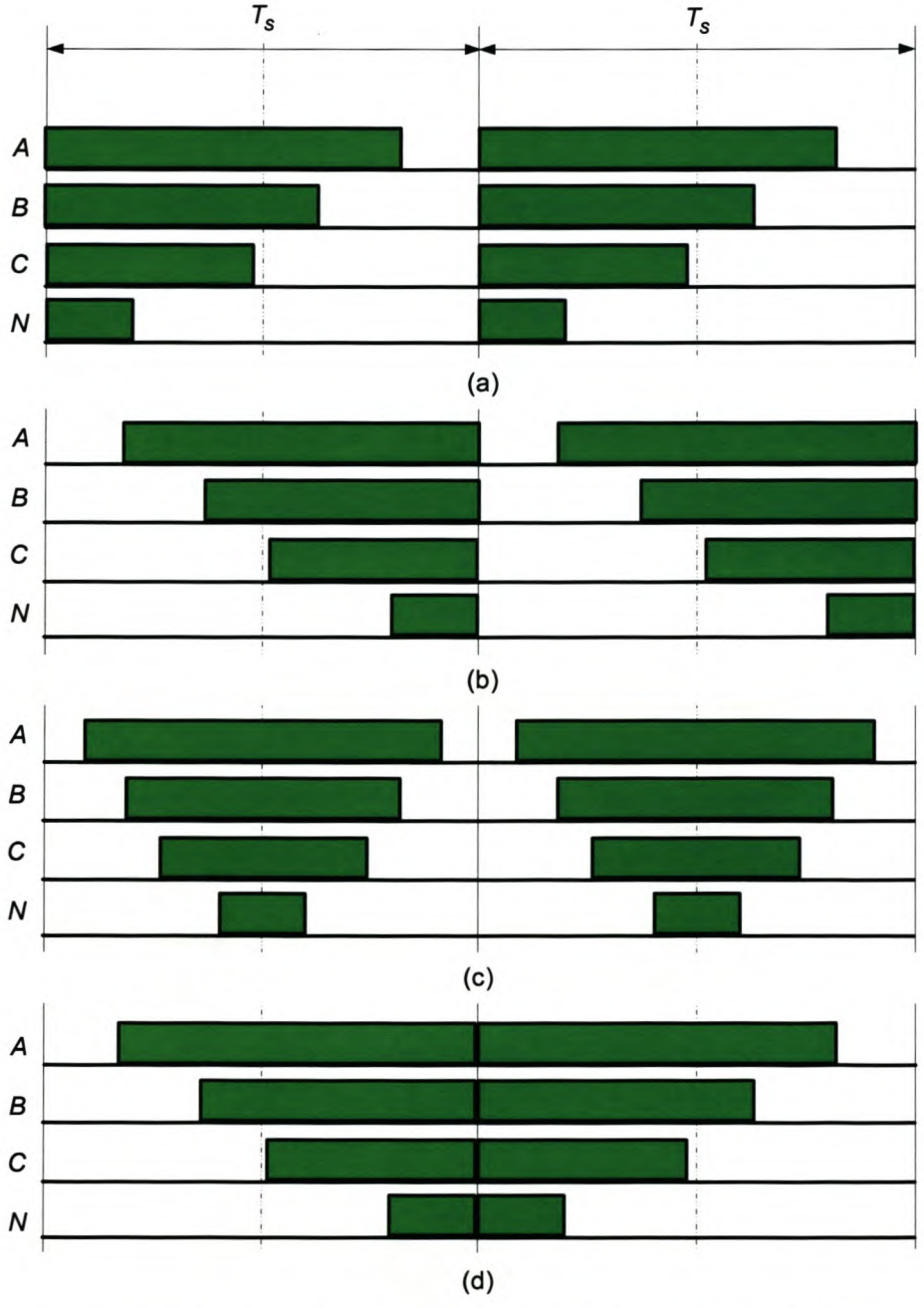


Figure 2-12 Category 1 switching schemes (a) Rising-edge aligned, (b) Falling-edge aligned, (c) Symmetrically aligned, (d) Alternative sequencing scheme

The rising-edge aligned and falling-edge aligned sequencing schemes, as shown in Figure 2-12, align respectively all the '0' to '1' transitions and the '1' to '0' transitions. The symmetrically aligned sequencing scheme produce the lowest output distortion and harmonic spectrum [7], and the alternative switching scheme provides the lowest switching losses of all the category 1 sequencing schemes.

Figure 2-13 illustrates the different sequencing schemes for category 2, when the reference vector lies in sector 1.

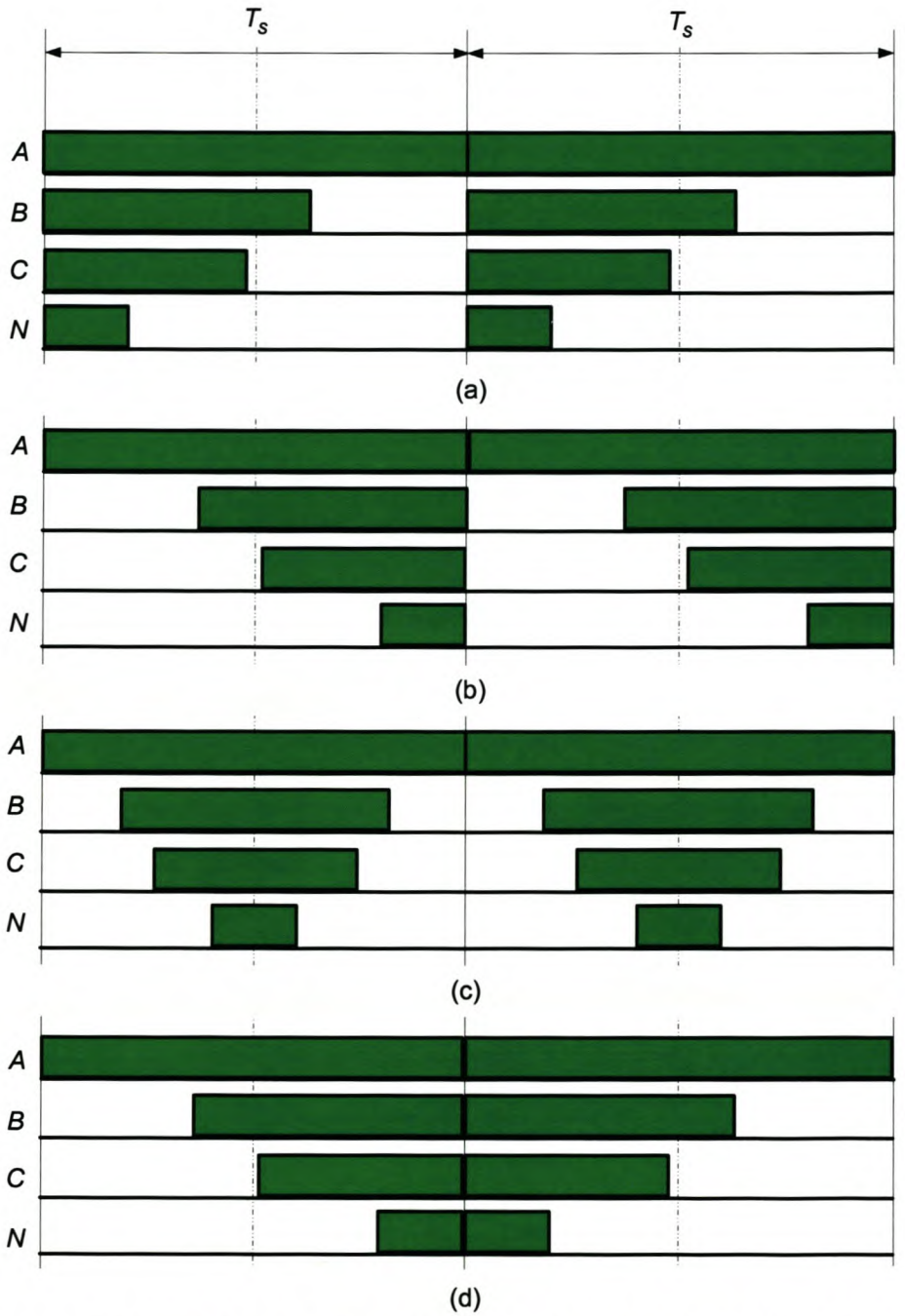


Figure 2-13 Category 2 switching schemes (a) Rising-edge aligned, (b) Falling-edge aligned, (c) Symmetrically aligned, (d) Alternative sequencing scheme

In high-power applications, power losses are of great concern. Category 2 sequencing schemes are minimum power-loss schemes since the phase which carries the highest current is not switched. Otherwise the sequencing schemes are similar to those of category 1, except that the harmonic content is higher in category 2 sequencing schemes.

A more detailed discussion of modulation schemes can be found in [16], [17].

This thesis will focus on the symmetrically aligned category 1 sequencing scheme in order to ensure the lowest output distortion and harmonic spectrum.

2.3 Development of a dynamic system model for a three-phase four-wire system

The development of a system model can be divided into two parts; the load side and the inverter side. The author in [12] proved that in the dq0 output space the inverter's leg voltages are the same as the load voltages. This proof will now be summarised in Section 2.3.1.

2.3.1 Representing the inverter output voltages in terms of the inverter leg voltages in the dqo output space

The following equation is obtained by transforming the load voltages V_{AN}, V_{BN}, V_{CN} and V_N to the dqo output space using the transformation matrix $\mathbf{T}_{dqoz}$:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \\ V_z \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \\ V_N \end{bmatrix} = \mathbf{T}_{dqoz} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \\ V_N \end{bmatrix} \tag{2-30}$$

and Equation (2-31) can be found from Figure 2-5:

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \\ V_N \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \\ V_g \end{bmatrix} = \mathbf{T}_{\ln 4} \begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \\ V_g \end{bmatrix} \tag{2-31}$$

where

$\mathbf{T}_{\ln 4}$ is the matrix that relates the load voltages to the leg voltages of the inverter

Substituting Equation (2-31) into Equation (2-30) the following equation is obtained:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \\ V_z \end{bmatrix} = T_{dqoz} T_{ln4} \begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \\ V_g \end{bmatrix} \tag{2-32}$$

The matrix $\begin{bmatrix} V_{Ag} & V_{Bg} & V_{Cg} & V_g \end{bmatrix}^T$ can also be represented in the dqo space:

$$\begin{bmatrix} V_d^* \\ V_q^* \\ V_0^* \\ V_z^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \\ V_g \end{bmatrix} = \mathbf{T}_{dqoz} \begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \\ V_g \end{bmatrix} \tag{2-33}$$

The inverse of $\mathbf{T}_{dqoz}$ can be used to determine the inverter leg voltages from their dqo output space representation as shown:

$$\begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \\ V_g \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \\ 0 & 0 & -\frac{3}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_d^* \\ V_q^* \\ V_0^* \\ V_z^* \end{bmatrix} = \left[T_{dqoz} \right]^{-1} \begin{bmatrix} V_d^* \\ V_q^* \\ V_0^* \\ V_z^* \end{bmatrix} \tag{2-34}$$

Substituting Equation (2-34) into Equation (2-32) the following is obtained:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \\ V_z \end{bmatrix} = T_{dqoz} T_{ln4} \left[T_{dqoz} \right]^{-1} \begin{bmatrix} V_d^* \\ V_q^* \\ V_0^* \\ V_z^* \end{bmatrix} \tag{2-35}$$

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \\ V_z \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & \sqrt{3} & 0 \end{bmatrix} \begin{bmatrix} V_d^* \\ V_q^* \\ V_0^* \\ V_z^* \end{bmatrix} \tag{2-36}$$

By disregarding V_Z, since it is only a mathematical fabrication, it can be seen from Equation (2-36) that in the dqo output space the inverters' leg voltages and the inverters' output voltages are the same.

2.3.2 The dynamic model of the three-phase four-wire topology

Ryan in [12], [39] and [40] analysed the single-phase full-bridge inverter topology and the three phase three-wire topology in order to extend the theory to analyze the three-phase four-wire topology.

Ryan concluded that, by comparing the dynamic models of the single-phase full-bridge inverter and the three-phase three-wire topology, the equivalent dynamic model of the three phase four-wire topology is as shown in Figure 2-14.

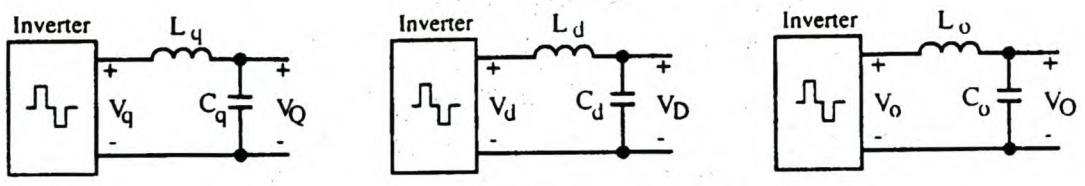


Fig. 2.32: Dynamic Models for 4-Leg UPS Inverter

Figure 2-14 The Dynamic model as proposed by [12]

with $L_a = L_b = L_c = L_d = L_q = L_o$ and $C_a = C_b = C_c = C_d = C_q = C_o$. *"As with the 3-leg inverter, the filter components in Figure. 2.32 are equivalent to the original components" [12]*

This statement is, however, not valid.

The rest of this section will prove the correct dynamic model of the three-phase four-wire topology. The dynamic model will be further expanded to include the equivalent series resistances of the inductors, as well as the effect of the neutral inductor.

Consider the circuit diagram shown in Figure 2-15.

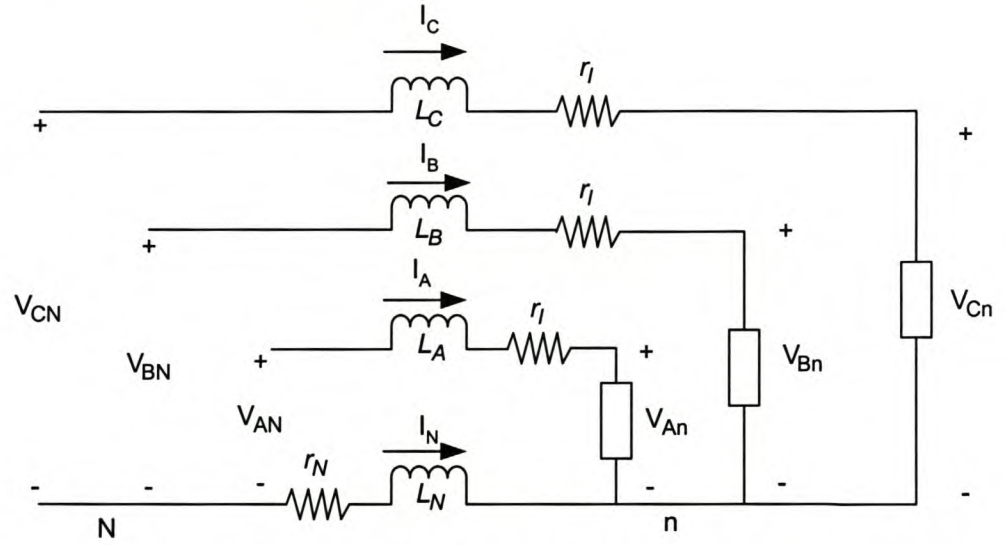


Figure 2-15 – Representation of the inductors connected between the load and the four-leg inverter

The following voltage loop equations can be obtained from Figure 2-15:

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \\ V_N \end{bmatrix} = \begin{bmatrix} L_A \frac{di_A}{dt} \\ L_B \frac{di_B}{dt} \\ L_C \frac{di_C}{dt} \\ 0 \end{bmatrix} + \begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \\ V_N \end{bmatrix} - \begin{bmatrix} L_N \frac{di_N}{dt} \\ L_N \frac{di_N}{dt} \\ L_N \frac{di_N}{dt} \\ 0 \end{bmatrix} - r_l \begin{bmatrix} i_A \\ i_B \\ i_C \\ 0 \end{bmatrix} - r_N \begin{bmatrix} i_N \\ i_N \\ i_N \\ 0 \end{bmatrix} \tag{2-37}$$

By letting $L_A = L_B = L_C = L$ Equation (2-37) can be transformed to the dqo space by using the transformation matrix T_{dqoz}:

$$\begin{bmatrix} V_d^* \\ V_q^* \\ V_0^* \\ V_z^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix} \left(L\frac{d}{dt}\begin{bmatrix} i_A \\ i_B \\ i_C \\ 0 \end{bmatrix} - L_N \frac{d}{dt}\begin{bmatrix} i_N \\ i_N \\ i_N \\ 0 \end{bmatrix} + r_l \begin{bmatrix} i_A \\ i_B \\ i_C \\ 0 \end{bmatrix} - r_l \begin{bmatrix} i_N \\ i_N \\ i_N \\ 0 \end{bmatrix} + \begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \\ V_{Nn} \end{bmatrix} \right) \tag{2-38}$$

However, it must be noted that the standard form of the transformation matrix utilised to transform the phase currents to the dq0 output space is as shown:

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \\ i_z \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \\ i_N \end{bmatrix} \tag{2-39}$$

Considering Equation (2-38) and Equation (2-39), it can be seen that the current matrixes in Equation (2-38) are not in the standard form to do a direct conversion. By using Equation (2-39) as a base, the phase currents can be calculated in the dq0 space.

The rest of this chapter explains the mathematics behind the transformation of the abcn dynamic space model into the dq0 dynamic space model.

First consider the section of Equation (2-38) shown in Equation (2-40) and the transformation matrix shown in Equation (2-39).

$$\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}\left(L\frac{d}{dt}\begin{bmatrix} i_A \\ i_B \\ i_C \\ 0 \end{bmatrix}\right) \tag{2-40}$$

By comparing Equation (2-40) and Equation (2-39) the following can be seen. The d-component and the q-component are similar to I_d and I_q defined by the transformation matrix given in Equation (2-39). This is, however, not the case for the zero sequence component since, in order to define I_o using the transformational matrix, the neutral current component must be taken into consideration. The neutral current component is not present in Equation (2-40), thus an alternative route must be taken to calculate the zero sequence component.

By calculating the third row of Equation (2-40) the following result can be obtained:

$$L\frac{d}{dt}\left(\sqrt{\frac{2}{3}}\frac{1}{2\sqrt{2}}(i_A + i_B + i_C)\right) \tag{2-41}$$

Noting that: $i_A + i_B + i_C = -i_N$ Equation (2-41) can be rewritten as follows:

$$L\frac{d}{dt}\left(\frac{1}{2\sqrt{3}}(-i_N)\right) \tag{2-42}$$

and from the transformation matrix shown in Equation (2-39), i_o and i_N are related as follows:

$$i_N = \sqrt{\frac{2}{3}}\left\{-\frac{3}{2\sqrt{2}}i_0 + \frac{\sqrt{3}}{2\sqrt{2}}i_z\right\} \tag{2-43}$$

Since from Equation (2-39) $i_z = 0$, Equation (2-43) can be simplified as shown:

$$i_N = -\frac{\sqrt{3}}{2}i_0 \tag{2-44}$$

Now substituting Equation (2-44) into Equation (2-42) the following result can be obtained:

$$L\frac{d}{dt}\left(\frac{1}{2\sqrt{3}}\left(\frac{\sqrt{3}}{2}i_0\right)\right) = \frac{L}{4}\frac{di_0}{dt} \tag{2-45}$$

This proves that Equation (2-40) can be represented in the dqo output space as:

$$\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}\left(L\frac{d}{dt}\begin{bmatrix} i_A \\ i_B \\ i_C \\ 0 \end{bmatrix}\right) = \begin{bmatrix} L\frac{d}{dt}i_d \\ L\frac{d}{dt}i_q \\ \frac{L}{4}\frac{d}{dt}i_0 \\ 0 \end{bmatrix} \tag{2-46}$$

The same method can be used to prove that:

$$\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}\left(r_l\begin{bmatrix} i_A \\ i_B \\ i_C \\ 0 \end{bmatrix}\right) = \begin{bmatrix} r_l i_d \\ r_l i_q \\ \frac{r_l}{4}i_0 \\ 0 \end{bmatrix} \tag{2-47}$$

The next part of Equation (2-38) that needs to be represented in the dqo space is:

$$\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}\left(L_N\frac{d}{dt}\begin{bmatrix} i_N \\ i_N \\ i_N \\ 0 \end{bmatrix}\right) \tag{2-48}$$

By doing matrix manipulations on Equation (2-48) the following result can be found:

$$\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}\left(L_N\frac{d}{dt}\begin{bmatrix} i_N \\ i_N \\ i_N \\ 0 \end{bmatrix}\right) = L_N\frac{d}{dt}\begin{bmatrix} 0 \\ 0 \\ \frac{\sqrt{3}}{2}i_N \\ 0 \end{bmatrix} \tag{2-49}$$

Substituting Equation (2-44) into Equation (2-49), the following result can be obtained in the dq0 output space as:

$$\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}\left(L_N \frac{d}{dt}\begin{bmatrix} i_N \\ i_N \\ i_N \\ 0 \end{bmatrix}\right) = L_N \frac{d}{dt}\begin{bmatrix} 0 \\ 0 \\ -\frac{3}{4}i_o \\ 0 \end{bmatrix} \tag{2-50}$$

The same method can be used to prove that:

$$\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix}\left(r_N \begin{bmatrix} i_N \\ i_N \\ i_N \\ 0 \end{bmatrix}\right) = r_N \begin{bmatrix} 0 \\ 0 \\ -\frac{3}{4}i_0 \\ 0 \end{bmatrix} \tag{2-51}$$

Once all the different sections have been transformed into the dq0 output space, the dynamic model can be calculated in the dq0 output space by substituting the results obtained from Equation (2-46), Equation (2-47), Equation (2-50) and Equation (2-51) into Equation (2-38):

$$\begin{aligned} \begin{bmatrix} V_d^* \\ V_q^* \\ V_0^* \\ V_z^* \end{bmatrix} &= L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ \frac{1}{4}i_o \\ 0 \end{bmatrix} + L_N \frac{d}{dt}\begin{bmatrix} 0 \\ 0 \\ \frac{3}{4}i_o \\ 0 \end{bmatrix} + r_l \begin{bmatrix} i_d \\ i_q \\ \frac{1}{4}i_o \\ 0 \end{bmatrix} + r_N \begin{bmatrix} 0 \\ 0 \\ \frac{3}{4}i_o \\ 0 \end{bmatrix} + \begin{bmatrix} V_d \\ V_q \\ V_o \\ V_z \end{bmatrix} \\ &= \frac{d}{dt}\begin{bmatrix} Li_d \\ Li_q \\ \left(L\frac{1}{4} + L_N\frac{3}{4}\right)i_o \\ 0 \end{bmatrix} + \begin{bmatrix} i_d \\ i_q \\ \left(r_l\frac{1}{4} + r_N\frac{3}{4}\right)i_o \\ 0 \end{bmatrix} + \begin{bmatrix} V_d \\ V_q \\ V_o \\ V_z \end{bmatrix} \end{aligned} \tag{2-52}$$

Finally Equation (2-52) can be written in the standard control canonical form:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \begin{bmatrix} -\frac{r_l}{L} & 0 & 0 \\ 0 & -\frac{r_l}{L} & 0 \\ 0 & 0 & -\frac{\left(r_l\frac{1}{4}+r_N\frac{3}{4}\right)}{\left(L\frac{1}{4}+\frac{3}{4}L_N\right)} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{L} & 0 & 0 \\ 0 & \frac{V_{dc}}{L} & 0 \\ 0 & 0 & \frac{V_{dc}}{\left(L\frac{1}{4}+\frac{3}{4}L_N\right)} \end{bmatrix}\begin{bmatrix} u_d \\ u_q \\ u_o \end{bmatrix} + \begin{bmatrix} -\frac{V_d}{L} \\ -\frac{V_q}{L} \\ -\frac{V_0}{\left(L\frac{1}{4}+\frac{3}{4}L_N\right)} \end{bmatrix} \tag{2-53}$$

where u_d, u_q and u_0 are the respective duty cycles for the d, q and o components.

By Letting $\mathbf{x} = \begin{bmatrix} x_1 & x_2 & x_3 \end{bmatrix}^T = \begin{bmatrix} i_d & i_q & i_0 \end{bmatrix}^T$, $\mathbf{u} = \begin{bmatrix} u_d & u_q & u_0 \end{bmatrix}^T$ and writing it in the general form, $\dot{\mathbf{x}} = \mathbf{Ax} + \mathbf{Bu} + \mathbf{G}$, produce the following matrixes:

$$\mathbf{A} = \begin{bmatrix} -\frac{r_l}{L} & 0 & 0 \\ 0 & -\frac{r_l}{L} & 0 \\ 0 & 0 & -\frac{\left(r_l \frac{1}{4} + r_N \frac{3}{4}\right)}{\left(L\frac{1}{4} + \frac{3}{4}L_N\right)} \end{bmatrix}, \mathbf{B} = \begin{bmatrix} \frac{V_{dc}}{L} & 0 & 0 \\ 0 & \frac{V_{dc}}{L} & 0 \\ 0 & 0 & \frac{V_{dc}}{\left(L\frac{1}{4} + \frac{3}{4}L_N\right)} \end{bmatrix} \text{ and } \mathbf{G} = \begin{bmatrix} -\frac{V_d}{L} \\ -\frac{V_q}{L} \\ -\frac{V_0}{\left(L\frac{1}{4} + \frac{3}{4}L_N\right)} \end{bmatrix} \quad \text{(2-54)}$$

2.4 Summary

Various power-circuit configurations were discussed, which are utilised in active harmonic compensation. A three-phase four-wire topology was developed in the dqo space, and a true three-dimensional space vector PWM scheme was developed.

The dynamic system model in the stationary dq0 space for the three-phase four-wire topology as proposed by [12] was proven incorrect, and the correct dynamic model was developed, which also takes the effect of the neutral inductor into consideration.

Chapter 3 will discuss the development of the reference signal-generating algorithms for shunt active power filters.

3. Reference signal-generating algorithms

3.1 Introduction

The development of the reference signal-generating algorithms for shunt active power filters will be discussed by firstly defining two different methods for generating the reference current signals. This will be followed by a prediction method that will enable the proper prediction of the reference currents in a three-phase four-wire system, and finally the two discussed reference signal-generating algorithms will be analysed under non-ideal conditions.

3.2 Generalised instantaneous reactive power theory

The first algorithm that will be discussed is the algorithm developed by Peng *et al.* in [18], which will be preceded by a brief history to explain the development of this algorithm.

Akagi *et al.* developed in [19] the instantaneous reactive power theory, which was defined on the basis of the instantaneous value concept for arbitrary voltage and current waveforms. This theory, however, is only valid for three-phase systems without zero sequence currents and voltages [20]. Willems then went ahead and proposed a power theory for polyphase systems, which includes three-phase systems with zero sequence components in [20]. His approach, however, was based on the decomposition of the currents into orthogonal current components, rather than power components [18], [21]. Peng *et al.* then developed the generalised instantaneous reactive power theory (GIRPT) in [18], which is valid for sinusoidal or non-sinusoidal, balanced or unbalanced three-phase systems, with or without zero-sequence currents and voltages.

The rest of this section will summarise Peng's theory.

$\mathbf{V_s}$ and $\mathbf{I_L}$ is defined using the transformation matrix T_{dqoz} defined in Equation (2-12), with the z component ignored.

$$\mathbf{V_s} = \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \mathbf{T}_{dqoz} \begin{bmatrix} v_a \\ v_b \\ v_c \\ v_n \end{bmatrix} \tag{3-1}$$

$$\mathbf{I_L} = \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \mathbf{T}_{dqoz} \begin{bmatrix} i_a \\ i_b \\ i_c \\ i_n \end{bmatrix} \tag{3-2}$$

From [18] the generalised instantaneous active power and the generalised instantaneous reactive power component can respectively be calculated as shown:

$$\begin{aligned} P_L &= \mathbf{V_s} \bullet \mathbf{I_L} \\ &= \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} \bullet \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \\ &= v_d i_d + v_q i_q + v_0 i_0 \end{aligned} \tag{3-3}$$

$$\begin{aligned} \mathbf{Q_L} &= \mathbf{V_s} \times \mathbf{I_L} \\ &= \begin{bmatrix} Q_{d-L} \\ Q_{q-L} \\ Q_{0-L} \end{bmatrix} \\ &= \begin{bmatrix} v_q i_0 - v_0 i_q \\ v_0 i_d - v_d i_0 \\ v_d i_q - v_q i_d \end{bmatrix} \end{aligned} \tag{3-4}$$

P_L and $\mathbf{Q_L}$ can further be divided into 2 components:

$$P_L = \bar{P}_L + \tilde{P}_L \tag{3-5}$$

$$Q_L = \bar{Q}_L + \tilde{Q}_L \tag{3-6}$$

where

$\bar{P}_L$ is the instantaneous active power component from the fundamental frequency under purely symmetrical conditions

$\tilde{P}_L$ is the instantaneous active power component from the harmonics and unsymmetries

$\bar{Q}_L$ is the instantaneous reactive power component from the fundamental frequency under purely symmetrical conditions

$\tilde{Q}_L$ is the instantaneous reactive power component from the harmonics and unsymmetries.

In order to isolate the fundamental and harmonic components a second order low-pass Butterworth filter is utilized with a 3db cut-off frequency of 20 Hz. The transfer function of this filter in the s-domain is given in Equation (3-7) [H6], and can be transformed to the z-domain by using a z-transform and a sampling frequency of 10 kHz.

$$G(s) = \frac{100}{6.331 \times 10^{-3} s^2 + 1.125 s + 100} \tag{3-7}$$

The difference equation can be calculated from the z-transformed transfer matrix as shown:

$$F_{out}[k] = 1.982 F_{out}[k-1] - 0.9824 F_{out}[k-2] + 7.851 \times 10^{-5} F_{in}[k-1] + 7.851 \times 10^{-5} F_{in}[k-2] \tag{3-8}$$

Once the desired active power and reactive power components are isolated, the current components can be calculated.

The instantaneous active power compensating current component and the instantaneous reactive power compensating current component can now be calculated using Equation (3-9) and Equation (3-10) respectively. P_C and $\mathbf{Q_C}$ are defined depending on which of the components in Equation (3-5) and Equation (3-6) must be compensated for.

$$\begin{aligned}\mathbf{I_{c\text{-}P}} &= \frac{P_C \mathbf{V_S}}{\mathbf{V_S} \cdot \mathbf{V_S}} \\ &= \frac{P_C \mathbf{V_S}}{V_d^2 + V_q^2 + V_0^2} \\ &= \frac{P_C}{V_d^2 + V_q^2 + V_0^2} \begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix}\end{aligned} \tag{3-9}$$

$$\begin{aligned}\mathbf{I_{c\text{-}Q}} &= \frac{\mathbf{Q_C} \times \mathbf{V_S}}{\mathbf{V_S} \cdot \mathbf{V_S}} \\ &= \frac{\mathbf{Q_C} \times \mathbf{V_S}}{V_d^2 + V_q^2 + V_0^2} \\ &= \frac{1}{V_d^2 + V_q^2 + V_0^2} \begin{bmatrix} Q_{C-q} V_0 - Q_{C-0} V_q \\ Q_{C-0} V_d - Q_{C-d} V_0 \\ Q_{C-d} V_q - Q_{C-q} V_d \end{bmatrix}\end{aligned} \tag{3-10}$$

Finally, the total compensating current , $\mathbf{I_c}$, that needs to be injected into the supply by the shunt active power filter is

$$\mathbf{I_c} = \mathbf{I_{c\text{-}P}} + \mathbf{I_{c\text{-}Q}} \tag{3-11}$$

3.3 Extended synchronous reference frame technique

The second algorithm that will be discussed is the extended synchronous reference frame technique. This theory is based on the theory proposed by Nabae *et al.* in [25]. This theory proposed a new definition of the instantaneous active-reactive current and power based on instantaneous space vectors in polar co-ordinates for three-phase three-wire topologies [25]. However, this theory does not address the effect of the zero-sequence current component. Gannett *et al.* in [33] discussed the effect of the zero-sequence current component in the synchronous reference frame technique; however, no documentation was found where a method was proposed to isolate the active and reactive power components from the zero-sequence current component using the synchronous reference frame technique. The isolation of the zero-sequence active and reactive power components is important because Akagi *et al.* proposed in [19] that the instantaneous reactive power component can be compensated for without energy storage components if the assumption is made that the converter switching devices are lossless.

Due to this shortcoming an extension will be proposed to the theory presented in [25] and [33], which will enable the isolation of the instantaneous active and reactive current components from the zero sequence current component.

Figure 3-1, Figure 3-2 and Figure 3-3 will be used to aid in the discussion of the proposed extended synchronous frame technique. Figure 3-1 shows the space vectors $\mathbf{V_s}$ and $\mathbf{I_L}$ in the dqo space, Figure 3-2 shows the top-view projection of Figure 3-1, and Figure 3-3 shows the side-view projection of Figure 3-1.

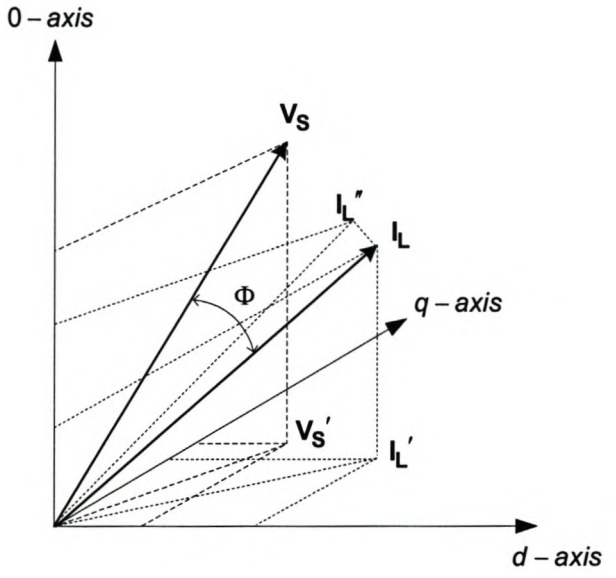


Figure 3-1 Voltage and current vector representation in rotating dq0 space

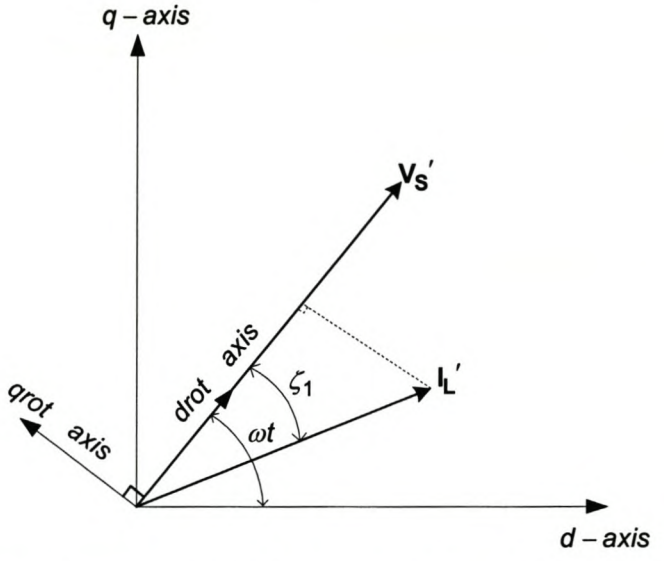


Figure 3-2 Voltage and current vector representation in rotating dq0 space (top view)

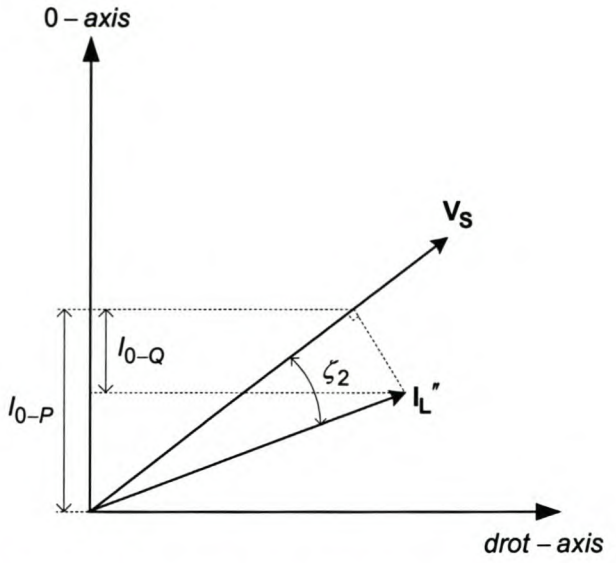


Figure 3-3 Voltage and current vector representation in rotating dq0 space

The current vector is transformed into the rotating dq0 space, as shown in Figure 3-2, by synchronizing the rotating dq0 space onto the projection of the supply voltage vector, $\mathbf{V_s}'$, using a phase lock loop and the transformation matrix shown:

$$\begin{bmatrix} i_{drot} \\ I_{qrot} \\ I_{0rot} \end{bmatrix} = \begin{bmatrix} \cos(\varpi t) & \sin(\varpi t) & 0 \\ -\sin(\varpi t) & \cos(\varpi t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{3-12}$$

In order to isolate the instantaneous active current and instantaneous reactive current component the definition of these components as proposed by Willems *et al.* in [20] will be used.

The current vector is split up into two components, orthogonal and parallel to the reference vector $\mathbf{V_s}$. The parallel current component, $\mathbf{I_P}$, can be defined as the instantaneous active current component, and the orthogonal component, $\mathbf{I_Q}$, can be defined as the instantaneous reactive current component. From Figure 3-1, Figure 3-2 and Figure 3-3 the instantaneous active current, $\mathbf{I_P}$, and the instantaneous reactive current, $\mathbf{I_Q}$, can respectively be found as shown:

$$\mathbf{I_P} = \left|\mathbf{I_L}'\right|\cos\left(\xi_1(t)\right) + \text{zero component of}\left\{\left|\mathbf{I_L}''\right|\cos\left(\xi_2(t)\right)\right\} \tag{3-13}$$

$$\mathbf{I_Q} = \left|\mathbf{I_L}'\right|\sin\left(\xi_1(t)\right) + \text{zero component of}\left\{\left|\mathbf{I_L}''\right|\sin\left(\xi_2(t)\right)\right\} \tag{3-14}$$

Equation (3-13) and Equation (3-14) can respectively be rewritten as shown (See Appendix B1 for the explanation):

$$\mathbf{I_P} = \mathbf{I_{drot}} + \frac{V_0 I_0}{V_{drot}^2 + V_0^2} \tag{3-15}$$

$$I_Q = I_{qrot} + \left(I_0 - \frac{V_0 I_0}{V_{drot}^2 + V_0^2} \right) \tag{3-16}$$

I_{drot} and I_{qrot} can further be decomposed into the following components:

$$I_{drot} = \bar{I}_{drot} + \tilde{I}_{drot} \tag{3-17}$$

$$I_{qrot} = \bar{I}_{qrot} + \tilde{I}_{qrot} \tag{3-18}$$

where

$\bar{I}_{drot}$ is the instantaneous active current component from the fundamental frequency under purely symmetrical conditions

$\tilde{I}_{drot}$ is the instantaneous active current component from the harmonics and unsymmetries

$\bar{I}_{qrot}$ is the instantaneous reactive current component from the fundamental frequency under purely symmetrical conditions

$\tilde{I}_{qrot}$ is the instantaneous reactive current component from the harmonics and unsymmetries.

3.4 Prediction of the reference current

Once the theoretical reference current signals have been determined, some factors must be taken into consideration to ensure that the reference current signals can be injected at the right time by the active filter. The rest of this section will discuss one of these factors and a possible solution will be provided.

The performance of an active filter is greatly deteriorated due to the time it takes to sample the current and voltage values, the time the DSP takes to process the sampled values and the switching action of the inverter. This can best be explained by considering Figure 3-4. At t=0 the currents and voltages are sampled. This takes a finite time and is represented by area (1). Once the values are sampled the DSP takes time to calculate the reference signals and the duty cycles for the voltage source inverter. This is represented by area (2). At $t=T_s$ the duty cycles are sent to the inverter to force the actual current to be the same as the reference current at $t=2T_s$. Thus the reference current is only realised after two switching periods. This effect is even more dramatic when relatively low switching frequencies are used [31].

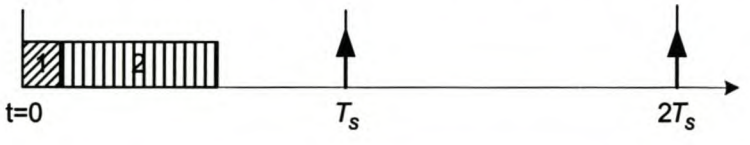


Figure 3-4 Explanation of time delay

Mattavelli in [30] proposed a method where the future value of the reference vector can be predicted. He stipulated that when the active filter is operational in steady state, the load current waveforms could be considered as periodic. Thus by rotating the reference vector in the dq plane at a selected angular velocity ω, as shown in Figure 3-2, the selected angular velocity, ω, component transforms to a DC component, which represents the angular frequency peak amplitude. This action is shown mathematically by:

$$\begin{bmatrix} i_{drot}(k) \\ I_{qrot}(k) \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \gamma \sin(\omega t) \\ -\gamma \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_d(k) \\ i_q(k) \end{bmatrix} \tag{3-19}$$

where

$\gamma = 1$ for all $3m+1$ orders of harmonic frequencies

$\gamma = -1$ for all $3m-1$ orders of harmonic frequencies

m= 0,1,2,3,...

To isolate the DC component a low-pass filter, as discussed in Section 3.2, can be used. A sine and cosine look-up table can then be implemented to predict the future value by adding or subtracting a phase shift component when the rotational current component is converted back to the stationary frame as shown:

$$\begin{bmatrix} i_d(k) \\ I_q(k) \end{bmatrix} = \begin{bmatrix} \cos(\omega t + \gamma\Delta\Phi) & -\gamma \sin(\omega t + \gamma\Delta\Phi) \\ \gamma \sin(\omega t + \gamma\Delta\Phi) & \cos(\omega t + \gamma\Delta\Phi) \end{bmatrix} \begin{bmatrix} i_{drot}(k) \\ i_{qrot}(k) \end{bmatrix} \tag{3-20}$$

where

$\gamma = 1$ for all $3m+1$ orders of harmonic frequencies

$\gamma = -1$ for all $3m-1$ orders of harmonic frequencies

m= 0,1,2,3,...

The direction of rotation is dependent on whether the isolated frequency component is a positive or negative sequence component. This direction is represented in Equation (3-20) by γ, and the time delay can be represented as:

$$\Delta\Phi = 1.5 * \frac{2\pi T_s}{T_f} \tag{3-21}$$

where

T_f is the period of the selected frequency component

T_s is the period of the switching frequency

The reason for the delay of 1.5 times is because a good approximation for space vector PWM is a half sample delay of a zero-order hold circuit. Adding the one switching period delay due to the sampling and computation time, it is found that the phase angle must be 1.5 times the switching period [34].

This technique, however, does not enable the prediction of the future zero-sequence current component because the zero-sequence current component exists in the stationary frame. The authors in [31] and [32] discussed a solution to compensate for the zero-sequence current component. They proposed the F-method, which uses a numerical implementation of a moving Fourier series to detect the harmonics of the reference current.

The F-method will now be discussed to predict the future zero-sequence current components.

The zero-sequence current components can be represented in a discrete system as shown:

$$I_{zero}(k) = \sum_{n=1}^{\infty}\left[a_n \cos(n\Omega k) + b_n \sin(n\Omega k)\right] \tag{3-22}$$

where:

$\Omega = \frac{2\pi}{N}$ and N being the number of samples during one fundamental period

a_n and b_n are the Fourier coefficients

n is the order of the harmonic frequency

The coefficients a_n and b_n can be written as shown:

$$a_n(k) = a_n(k-1) + \frac{4}{N}\left(I_{zero}(k) + I_{zero}\left(k - \frac{N}{2}\right)\right)\cdot\cos(n\Omega k) \tag{3-23}$$

$$b_n(k) = b_n(k-1) + \frac{4}{N}\left(I_{zero}(k) + I_{zero}\left(k - \frac{N}{2}\right)\right)\cdot\sin(n\Omega k) \tag{3-24}$$

In order to calculate the predicted zero sequence current value the angle by which the reference value must be phase shifted is added:

$$I_{zero(n)}(k+1) = a_n \cos(n\Omega k + \Delta\Phi_{zero}) + b_n \sin(n\Omega k + \Delta\Phi_{zero}) \tag{3-25}$$

where

$$\Delta\Phi_{zero} = 1.5 * \frac{2\pi n}{N}$$

Since $I_{zero}(k)$ is a symmetrical function, the response time of the F-method is half a cycle [32]. The complete process is illustrated in Figure 3-5.

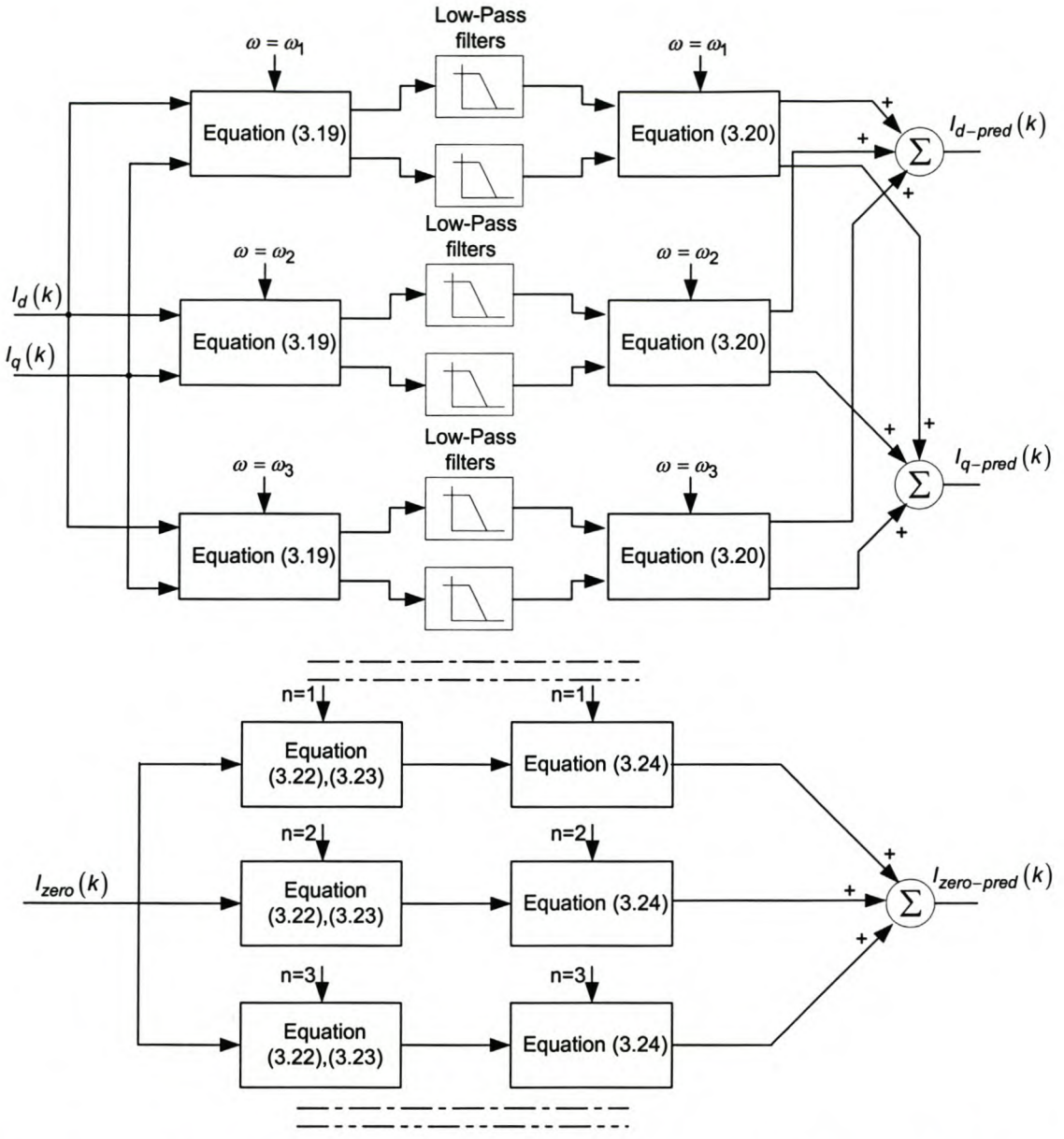


Figure 3-5 The complete process for predicting the future value of the reference vector

This method works satisfactorily, but it must be noted that it requires substantial computational effort from the DSP.

3.5 Comparison between the generalised instantaneous reactive power theory and synchronous reference frame technique

The proposed techniques discussed in Section 3.2.1 and Section 3.2.2 will now be investigated when implemented in a three-phase four-wire configuration under non-ideal conditions. The three-phase four-wire network that will be investigated is shown in Figure 3-6. In order to exclude external effects, the source inductance is ignored and the compensated source current will be determined by subtracting the compensating current from the load current.

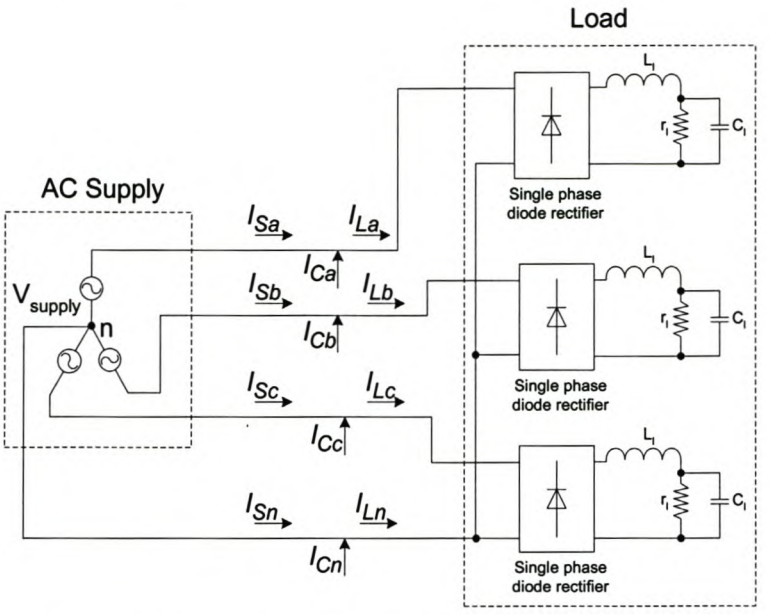


Figure 3-6 Three-phase four-wire network used for simulation studies

Under ideal conditions the two reference signal-generating topologies produce similar results. Figure 3-7 (a), (b), (c) and (d) show the uncompensated phase A load current, phase A compensating current, phase A compensated source current, and the neutral current before and after compensation under ideal conditions respectively.

In addition, the effects of non-ideal conditions such as supply voltage unbalance, supply voltage distortion and load unbalance will be investigated. The investigation will focus on the effect these have on the ability to ensure that the currents drawn by the supply are balanced and contain only the fundamental frequency component.

Lastly the two discussed reference current-generating topologies' ability to compensate only for reactive power is investigated.

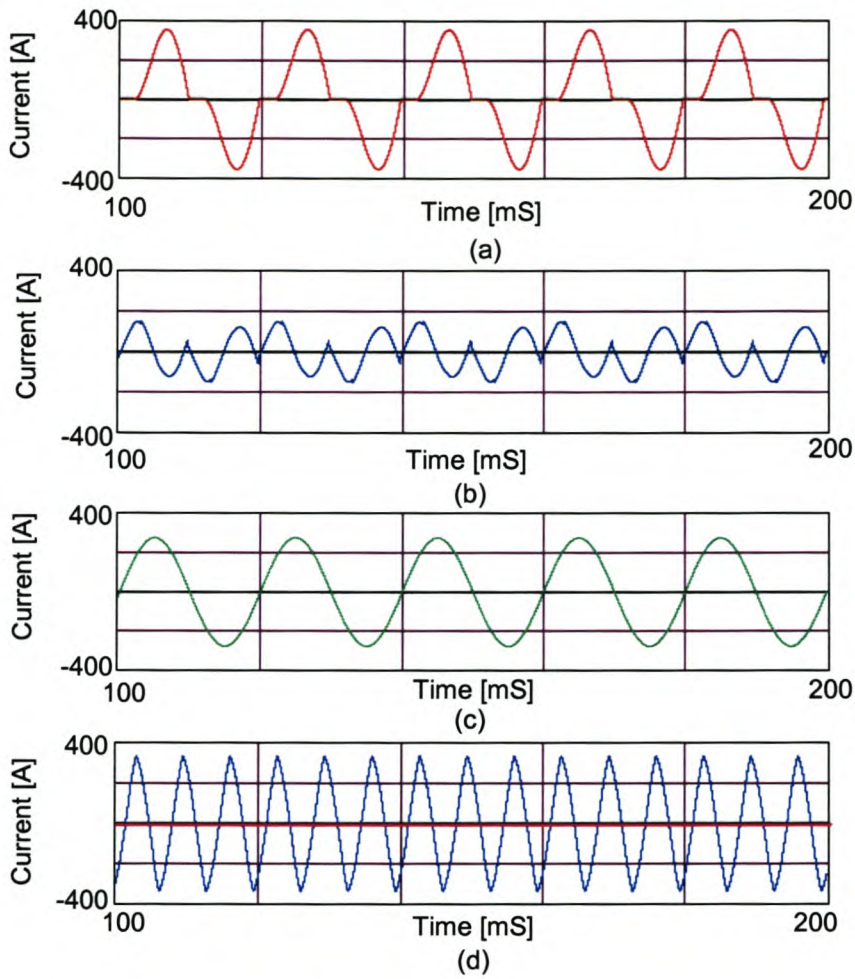


Figure 3-7 Ideal condition waveforms (equivalent for both reference algorithms) (a) Phase A load current, (b) Phase A compensating current, (c) Phase A compensated source current, (d) Neutral current with (magenta trace) and without (blue trace) compensation

3.5.1 Voltage Unbalance

The 15% unbalance, which was used between the supply voltage phases, as shown in Figure 3-8 (a), led to a load current unbalance of 15.2%. By using the GIRPT the source current after compensation, shown in Figure 3-8 (b), produced a zero sequence and negative sequence current unbalance of 3.4% and 1% respectively. The extended synchronous reference frame technique, shown in Figure 3-8 (c), gives a zero sequence and negative sequence current unbalance of 0% and 0.4% respectively after compensation. A summary of the results is given in Figure 3-9.

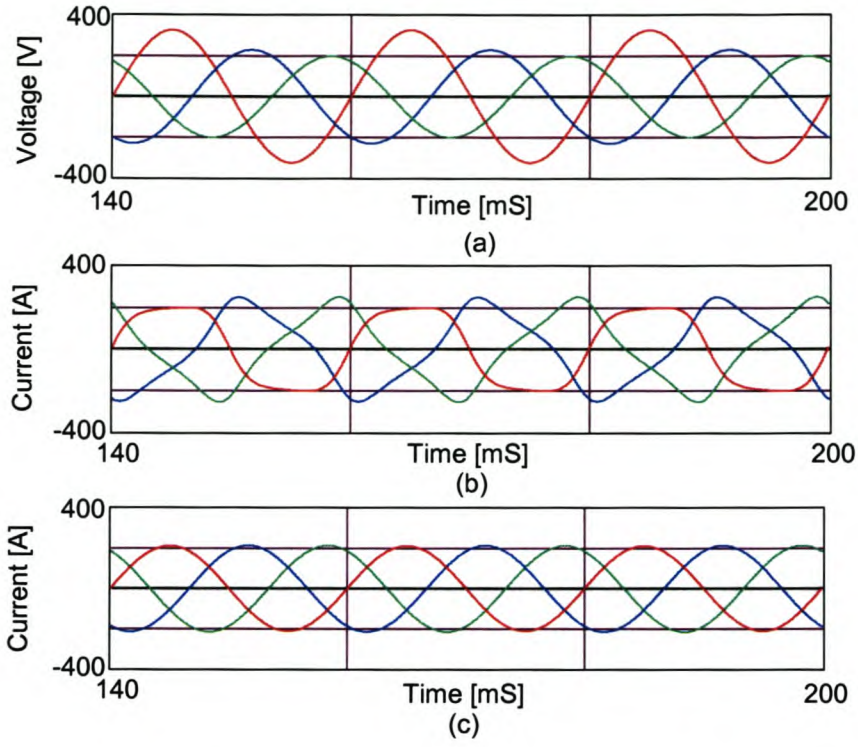


Figure 3-8 (a) Supply voltage unbalance, (b) Compensated source currents using GIRPT, (c) Compensated source currents using synchronous reference frame technique

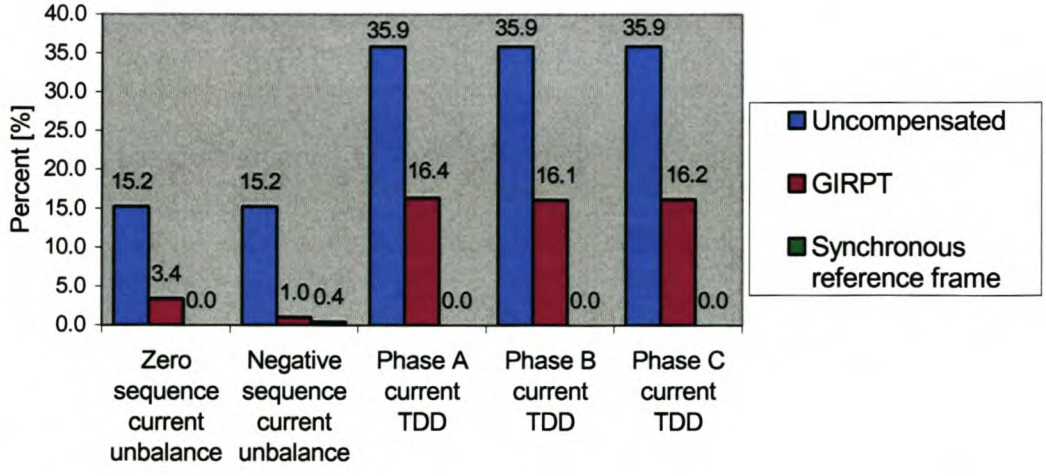


Figure 3-9 Summary of the results under unbalanced supply voltage conditions

3.5.2 Voltage distortion

To evaluate the effect of voltage distortion on the compensating currents a 10% 5th harmonic and a 5% 7th harmonic are added to the phase A supply voltage, as shown in Figure 3-10 (a). The uncompensated load current has a TDD of 28.4% and after compensation using the GIRPT technique the TDD is found to be 5.1%. By using the synchronous reference frame technique, the compensated source current after compensating is found to be 0%. These results are summarized in Figure 3-11.

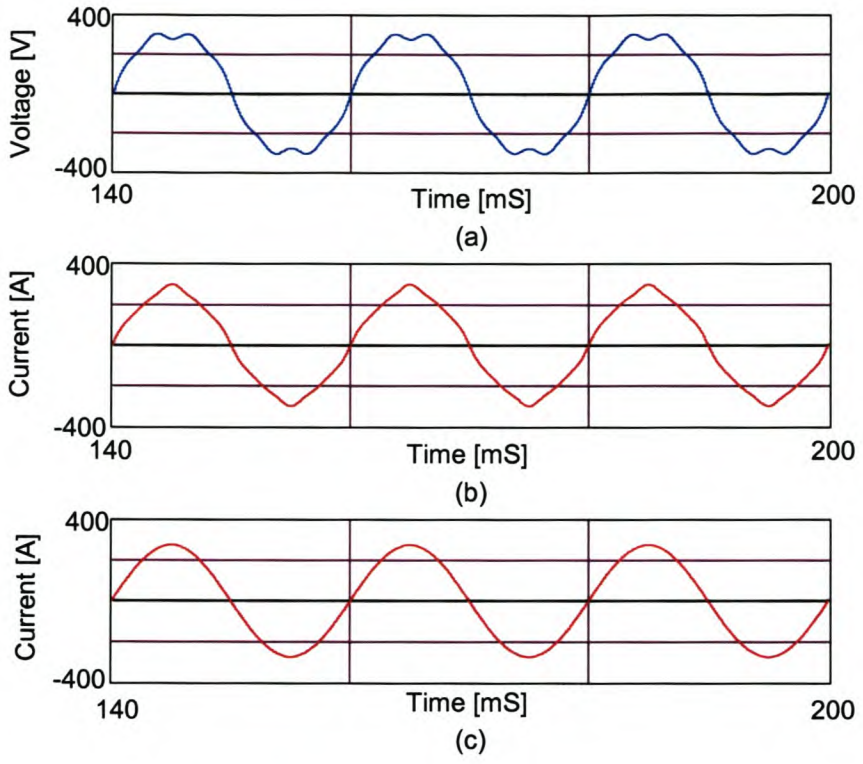


Figure 3-10 a) Phase A supply voltage distortion, (b) Compensated phase A source current using GIRPT, (c) Compensated phase A source current using Synchronous reference frame technique

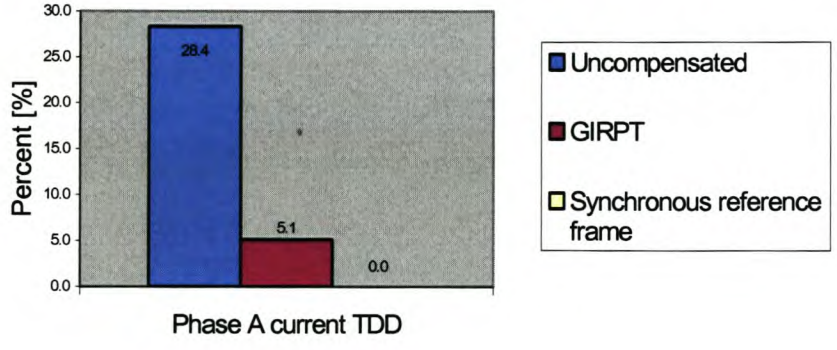


Figure 3-11 Summary of the results when the supply voltage is distorted

3.5.3 Load unbalance

To evaluate the effect when the load is unbalanced, two phase loads were disconnected, as shown in Figure 3-12 (a), to give an unbalance of 100%. By using the GIRPT the source current after compensation, shown in Figure 3-12 (b), gives a zero-sequence and negative sequence current unbalance of 0.02% and 2.71% respectively. The extended synchronous reference frame technique, shown in Figure 3-12 (c), gives a zero-sequence and negative-sequence current unbalance of 0.03% and 2.72% respectively after compensation. A summary of the results is given in Figure 3-14.

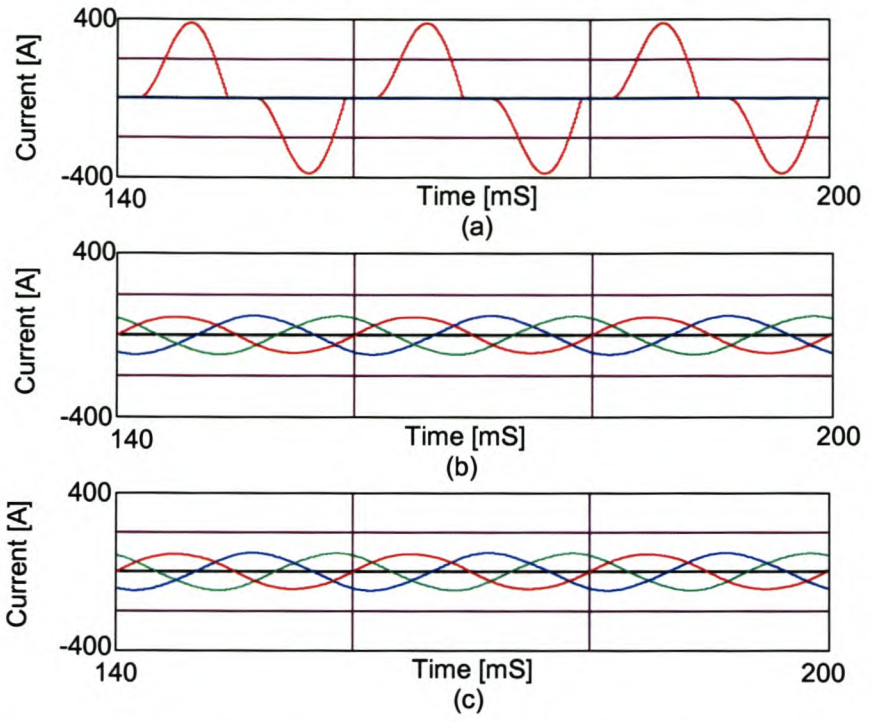


Figure 3-12 3-13 a) Phase A load current, Phase B and C =0, (b) Compensated source currents using GIRPT, (c) Compensated source currents using synchronous reference frame technique

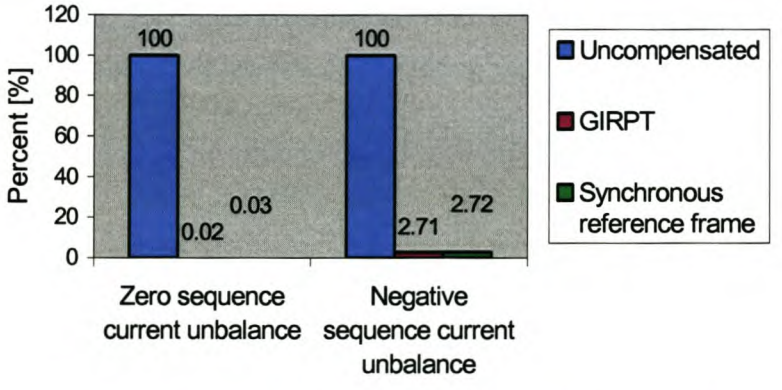


Figure 3-14 Summary of the results when there is a 100% load unbalance

3.5.4 Reactive power compensation

The ability to achieve reactive power compensation is shown in Figure 3-15. Figure 3-15 (a) shows the phase A supply voltage as well as the uncompensated load current. Figure 3-15 (b) shows the phase A supply voltage and the compensated phase A supply current using the GIRPT, and Figure 3-15 (c) shows the phase A supply voltage and the compensated phase A supply current using the proposed extended synchronous reference frame technique.

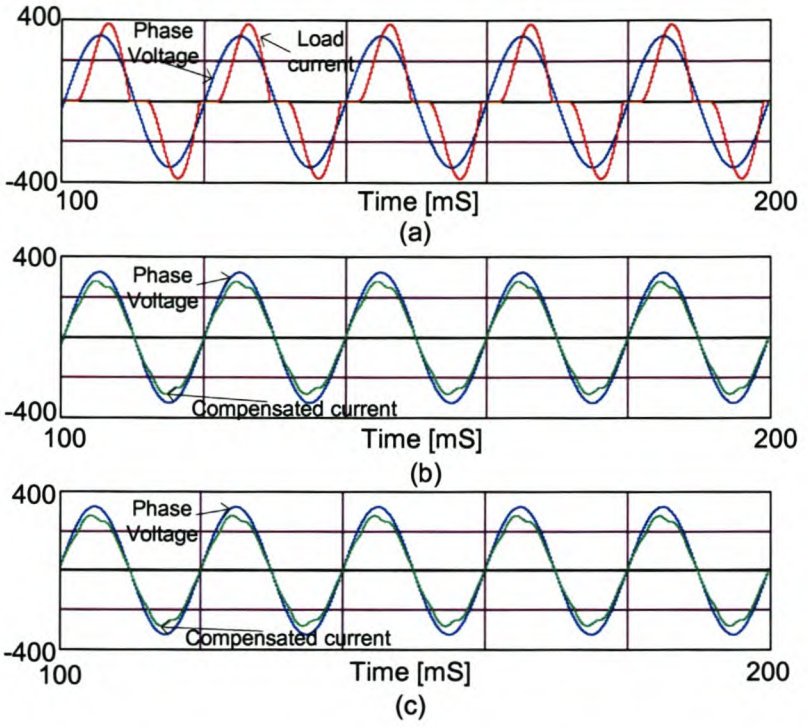


Figure 3-15 –Reactive power compensation (a) uncompensated phase A load current and supply voltage, (b) compensated phase A source current and supply voltage using GIRPT, (c) compensated phase A source current and supply voltage using the proposed extended synchronous reference frame technique

3.6 Summary

Two reference signal-generating algorithms were discussed.

The synchronous reference frame technique proposed by [25] was expanded to enable the separation of the zero-sequence current component into its instantaneous active and reactive current components.

A prediction method was proposed that will enable the proper prediction of the reference currents in a three-phase four-wire system, and the two discussed reference signal generating algorithms was analysed under non-ideal conditions.

From the simulation results it is concluded that when the supply voltages is unbalanced or distorted, the synchronous reference frame technique offer far more superior results than the generalised reactive power theory. The two discussed methods offer similar results when the load is unbalanced.

The rest of this thesis will employ the synchronous reference frame technique to generate the reference current signals.

Chapter 4 will discuss in detail the design process for the current controllers utilised to achieve proper reference current tracking.

4. Reference signal-tracking algorithms

4.1 Introduction

Active filters pose challenging problems for voltage source inverters mainly due to the fact that the reference currents contain a significantly, high harmonic content and sudden slope variations. These factors contribute to the challenging design of the control and practical implementation of active power filters [26].

It is the aim of this chapter to discuss in detail the design process for the current controllers utilised to achieve proper reference current tracking. Two categories of current controllers will be investigated, namely predictive current controllers and sliding mode current controllers.

Simulation results will be provided for the discussed current controllers under ideal conditions (i.e. no time delay and no dead-time effects), in order to focus on the current controller's ability to achieve proper reference current tracking. In chapter 5, a detail analysis will be done on the simulation results for the different current controllers with non-ideal effects incorporated.

4.2 Predictive current control

A predictive current controller works on the basis that it uses a dynamic model of the system to calculate once every sample period T_s a voltage vector $\mathbf{u}_{ref}$, which will force the line current vector to the reference current vector at the end of the sample period T_s.

The inverter DC-bus voltage, V_{dc} and the EMF voltage are assumed to be constant during the sampling period. The calculated reference vector, $\mathbf{u}_{ref}$, is then implemented in a modulating algorithm such as the three-dimensional space vector PWM modulating strategy discussed in Section 2.2.3.1.

In order to calculate the reference vector, consider the dynamic model as given in Equation (2-53):

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \begin{bmatrix} -\frac{r_l}{L} & 0 & 0 \\ 0 & -\frac{r_l}{L} & 0 \\ 0 & 0 & -\frac{\left(r_l\frac{1}{4}+r_N\frac{3}{4}\right)}{\left(L\frac{1}{4}+\frac{3}{4}L_N\right)} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{L} & 0 & 0 \\ 0 & \frac{V_{dc}}{L} & 0 \\ 0 & 0 & \frac{V_{dc}}{\left(L\frac{1}{4}+\frac{3}{4}L_N\right)} \end{bmatrix}\begin{bmatrix} u_d \\ u_q \\ u_o \end{bmatrix} + \begin{bmatrix} -\frac{V_d}{L} \\ -\frac{V_q}{L} \\ -\frac{V_0}{\left(L\frac{1}{4}+\frac{3}{4}L_N\right)} \end{bmatrix} \tag{4-1}$$

The differential term in Equation (4-1) can be approximated using the forward rectangular version of Euler's method [H5] as shown:

$$\frac{d}{dt}I_x = \frac{I_x(k+1)-I_x(k)}{T_s} \tag{4-2}$$

where

x represents the d, q and 0 components

$I_x(k+1)$ is the reference current component

$I_x(k)$ is the inverter's sampled current value

From Equation (4-1) and Equation (4-2) the following can be obtained:

$$\frac{I_{d-ref} - I_d(k)}{T_s} = -\frac{r_l}{L} I_d(k) + \frac{V_{dc}(k)}{L} u_d - \frac{V_d(k)}{L} \tag{4-3}$$

$$\frac{I_{q-ref} - I_q(k)}{T_s} = -\frac{r_l}{L} I_q(k) + \frac{V_{dc}(k)}{L} u_q - \frac{V_q(k)}{L} \tag{4-4}$$

$$\frac{I_{0-ref} - I_0(k)}{T_s} = -\frac{(0.25r_l + 0.75r_N)}{(0.25L + 0.75L_N)} I_0(k) + \frac{V_{dc}(k)}{(0.25L + 0.75L_N)} u_0 - \frac{V_0(k)}{(0.25L + 0.75L_N)} \tag{4-5}$$

Finally, by rearranging Equation (4-3) to (4-5) the equations to calculate the reference vector components can be determined as shown:

$$u_d = \frac{1}{V_{dc}(k)} \left\{ \frac{L\left(I_{d-ref} - I_d(k)\right)}{T_s} + r_l I_d(k) + V_d(k) \right\} \tag{4-6}$$

$$u_q = \frac{1}{V_{dc}(k)} \left\{ \frac{L\left(I_{q-ref} - I_q(k)\right)}{T_s} + r_l I_q(k) + V_q(k) \right\} \tag{4-7}$$

$$u_0 = \frac{1}{V_{dc}(k)} \left\{ \frac{(0.25L + 0.75L_N)\left(I_{0-ref} - I_0(k)\right)}{T_s} + (0.25r_l + 0.75r_N) I_0(k) + V_0(k) \right\} \tag{4-8}$$

The next section will show simulation results using Simplorer® version 4.2 for the discussed predictive current controller.

4.2.1 Simulation results

The simulation results seen in Figure 4-1 and Figure 4-2 are the results from the simulation setup as shown in Appendix C1. In order to evaluate only the performance of the predictive current controller the time delay and dead-time are set to 0 in the simulation.

Figure 4-1 (a) and Figure 4-2 (a) show the reference currents (black traces) and the actual currents (coloured traces) regulated by the inverter. The reference current components for Figure 4-1 (a) and Figure 4-2 (a) are respectively:

$$\begin{aligned} I_a &= 60\sin(\omega t) \\ I_a &= 40\sin(\omega t + 120^\circ) \\ I_a &= 20\sin(\omega t + 240^\circ) \end{aligned} \tag{4-9}$$

In Figure 4-1 (b) and Figure 4-2 (b) the reference current components are square waves with the phase current amplitudes for phase A = 40A, phase B = 30A and phase C = 20A.

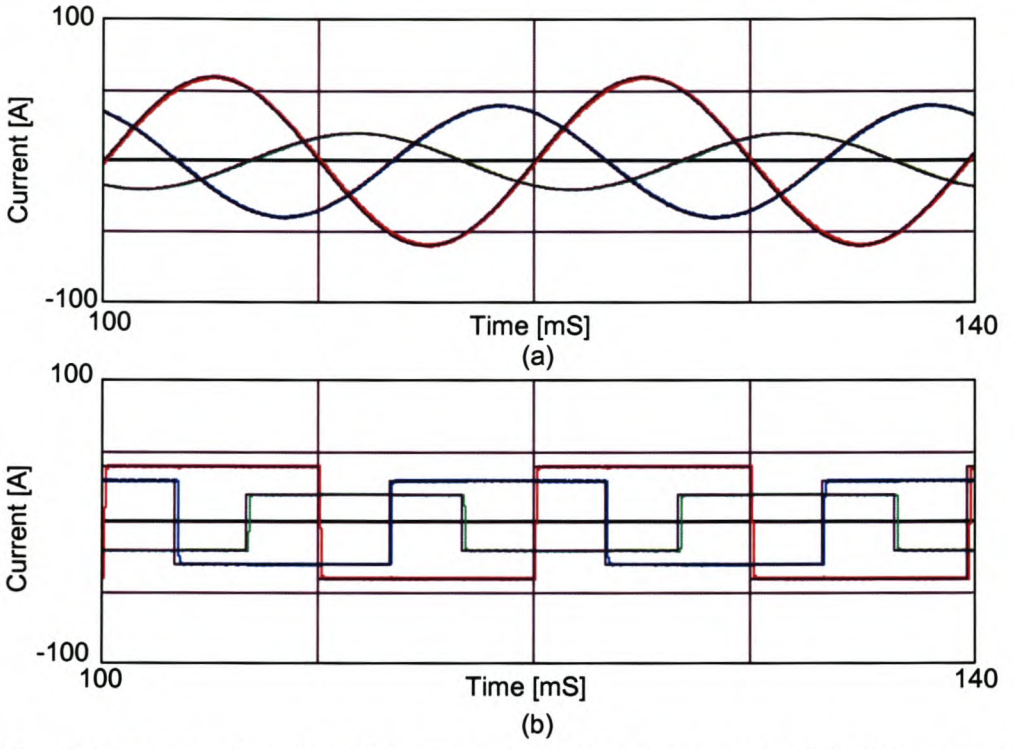


Figure 4-1 Predictive current control with neutral inductor not connected (a) 50 Hz sinusoidal, and (b) 50 Hz square waveforms

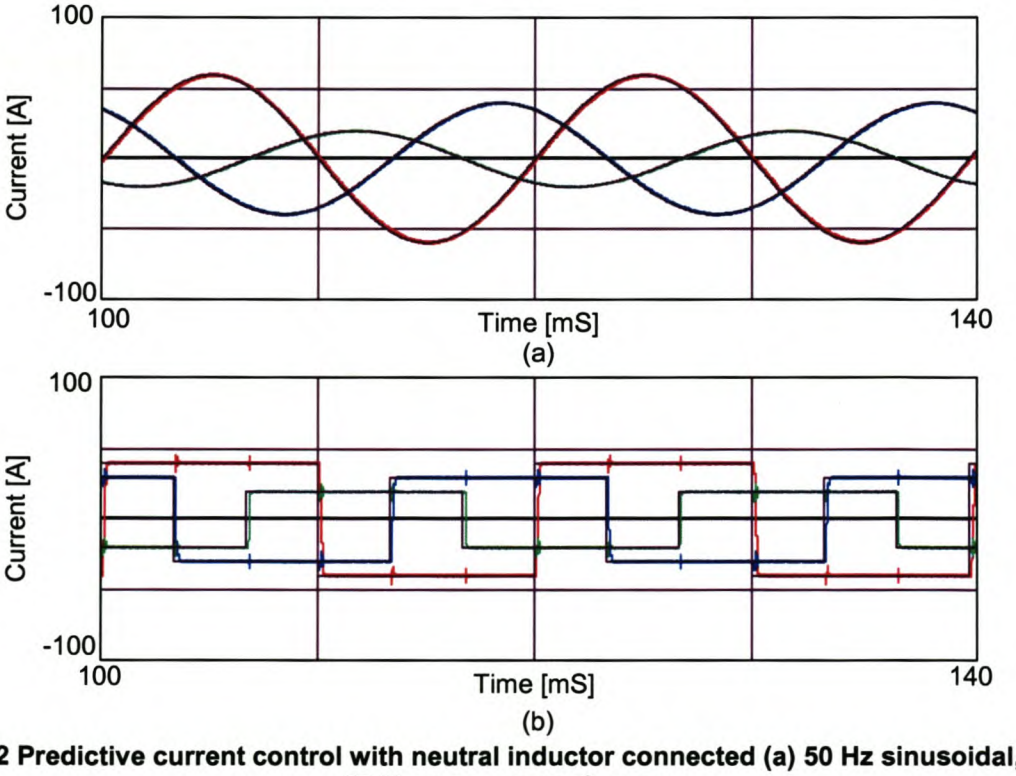


Figure 4-2 Predictive current control with neutral inductor connected (a) 50 Hz sinusoidal, and (b) 50 Hz square waveforms

As can be seen from these figures, the reference current tracking algorithms work satisfactorily with or without the neutral inductor connected. However in Figure 4-2 (b) glitches can be seen when there is a sudden step change in the reference current component. This can be attributed to the extra voltage drop across the neutral inductor that causes the reference voltage vector to lie outside the linear operating region of the inverter.

4.3 Variable structure control

4.3.1 Introduction

One major disadvantage of predictive current controllers is that their performance is highly dependant on the accurateness of the system model parameters. In a practical system the parameters are frequency dependant. Due to this frequency dependency variable structure controllers will be investigated, since this type of controllers is known for their robustness to parameter variations and its simplicity [41], [H8].

The typical inductance and equivalent series resistance values for an 800 µH inductor are shown in Figure 4-3 and Figure 4-4 respectively.

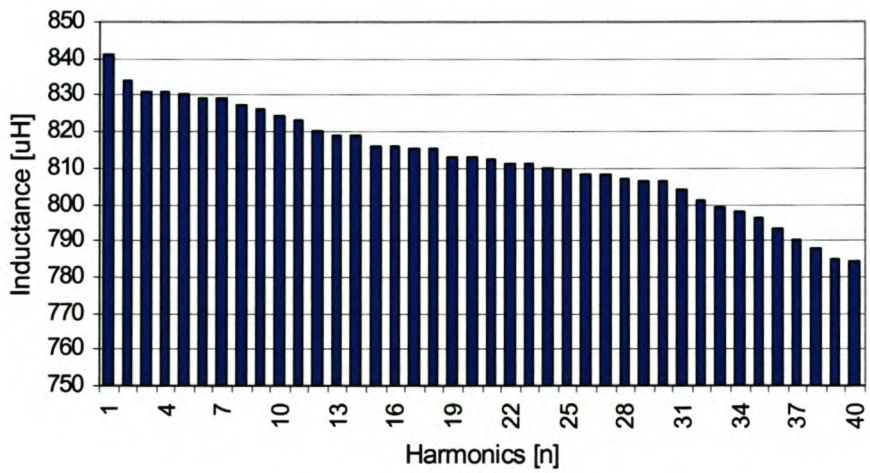


Figure 4-3 Equivalent inductance values for an 800 µH inductor

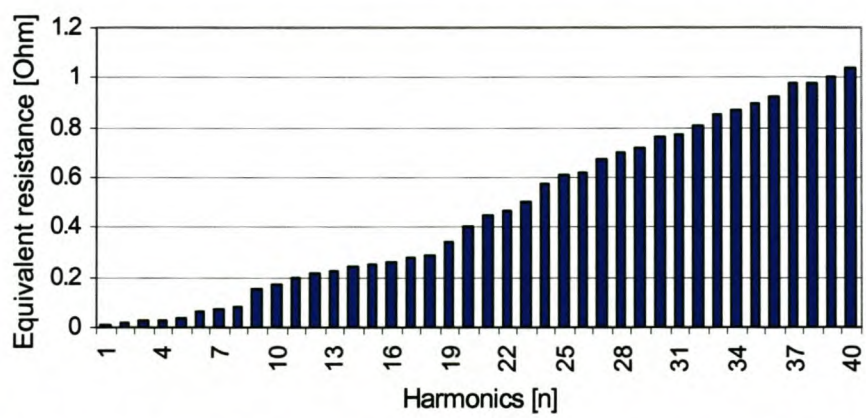


Figure 4-4 Equivalent resistance values for an 800 µH inductor

A brief overview will now be given of sliding mode current controllers.

Sliding mode controllers can be divided into two modes, namely, the reaching mode, which can be considered as a non-sliding mode, and the sliding mode. The reaching mode refers to when the trajectory is not on the switching function. When the trajectory is not on the switching function, a reaching control law $(\mathbf{u}_s)$ is employed to force the trajectory onto the switching function. Once the trajectory is on the switching function, i.e. sliding mode, the equivalent control $(\mathbf{u}_{eq})$ forces the trajectory towards the zero equilibrium point. This process is illustrated in Figure 4-5.

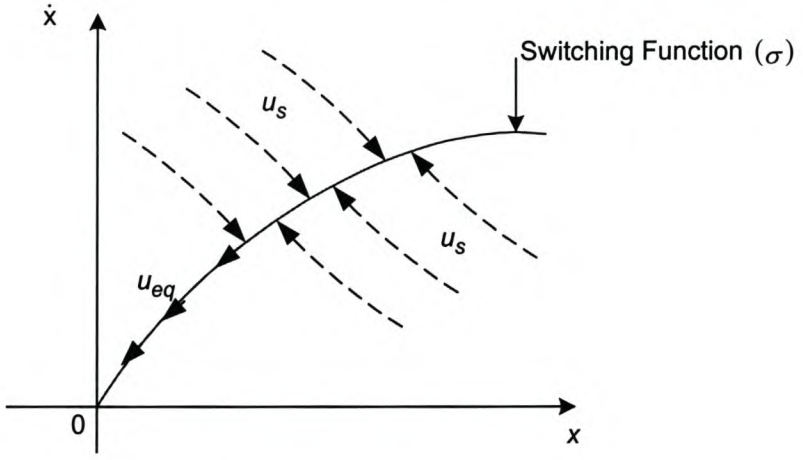


Figure 4-5 Explanation of sliding mode control

This control scheme can be summarised as a class of systems whereby the control law is deliberately changed during the control process according to some defined rules that depend on the state of the system [H9]. Figure 4-6 illustrates the basic structure of the sliding mode current control scheme.

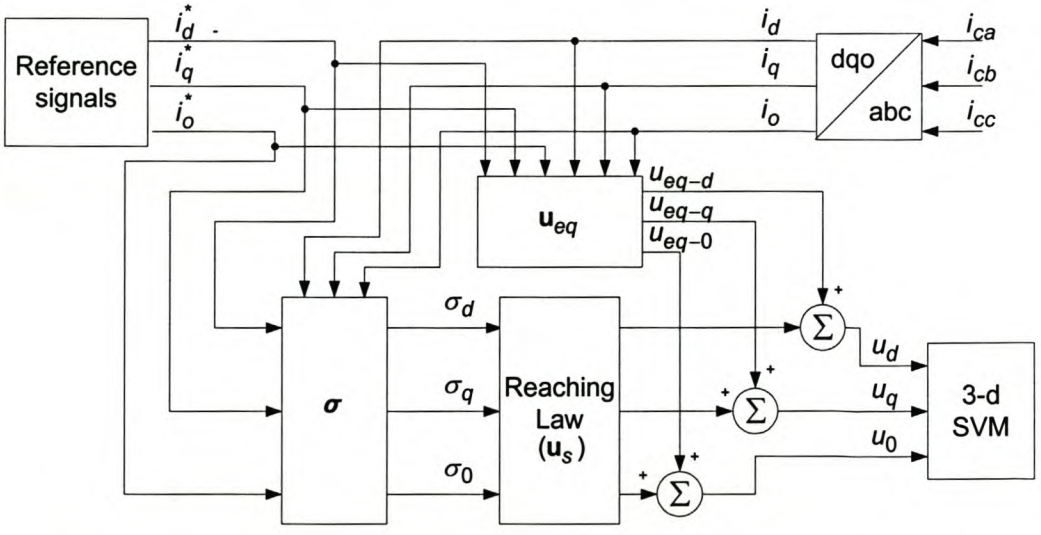


Figure 4-6 Control scheme outline of the proposed sliding mode controller

4.3.2 The switching function

The first step of the design process is determining the sliding mode switching function. The switching function that is chosen for this specific application is:

$$\boldsymbol{\sigma}(\mathbf{x}) = \begin{bmatrix} \sigma_d \\ \sigma_q \\ \sigma_0 \end{bmatrix} = \mathbf{K}(\mathbf{x}^* - \mathbf{x}) = \begin{bmatrix} k_1(x_1^* - x_1) \\ k_1(x_2^* - x_2^*) \\ k_2(x_3^* - x_3) \end{bmatrix} = \begin{bmatrix} k_1 & 0 & 0 \\ 0 & k_1 & 0 \\ 0 & 0 & k_2 \end{bmatrix} \begin{bmatrix} x_1^* - x_1 \\ x_2^* - x_2 \\ x_3^* - x_3 \end{bmatrix} \tag{4-10}$$

where

$\mathbf{x}^*$ is the reference state vector

Once the switching function is obtained, the next step in the design process is the design of the control law, $\mathbf{u}$. The control law, $\mathbf{u}$, can be rewritten in the following form:

$$\mathbf{u} = \mathbf{u_{eq}} + \mathbf{u_s}$$

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \begin{bmatrix} u_{eq-d} \\ u_{eq-q} \\ u_{eq-0} \end{bmatrix} + \begin{bmatrix} u_{s-d} \\ u_{s-q} \\ u_{s-0} \end{bmatrix} \tag{4-11}$$

where

$\mathbf{u}_s$ is the reaching law and guarantees the existence of the sliding mode

$\mathbf{u}_{eq}$ is the equivalent control and is only valid on the switching function

The next section will discuss the design process for the equivalent control.

4.3.3 Equivalent control

The existence of the equivalent control is a necessary condition to ensure the sliding motion over the switching function $\boldsymbol{\sigma}(\mathbf{x}) = 0$. In order to keep the state variables on the sliding function, the time derivative of $\boldsymbol{\sigma}(\mathbf{x})$ evaluated along the trajectory must be zero. Hence from Equation (4-10) and Equation (2-54):

$$\dot{\boldsymbol{\sigma}}(\mathbf{x}) = \mathbf{K}\left(\dot{\mathbf{x}}^* - \dot{\mathbf{x}}\right) = \mathbf{K}\dot{\mathbf{x}}^* - \mathbf{K}\left(\mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} + \mathbf{G}\right) = 0 \tag{4-12}$$

When $\mathbf{u} = \mathbf{u}_{eq}$ the equation for the equivalent control can be calculated from Equation (4-12):

$$\mathbf{u}_{eq} = -(\mathbf{K}\mathbf{B})^{-1}\mathbf{K}\left\{\mathbf{A}\mathbf{x} + \mathbf{G} - \dot{\mathbf{x}}^*\right\} \tag{4-13}$$

The respective components for $\mathbf{u}_{eq}$ can now be determined by using the model parameters as shown in Equation (2-54):

$$u_{eq-d} = \frac{\left(r_l x_1 + V_d + L\dot{x}_1^*\right)}{V_{dc}} \tag{4-14}$$

$$u_{eq-q} = \frac{\left(r_l x_2 + V_d + L\dot{x}_2^*\right)}{V_{dc}} \tag{4-15}$$

$$u_{eq-0} = \frac{\left(0.25r_l + 0.75r_N\right)x_3 + V_0 + \left(0.25L + 0.75L_N\right)\dot{x}_3^*}{V_{dc}} \tag{4-16}$$

4.3.4 Reaching mode

To ensure that the trajectory stays on the switching function, and thus an ideal sliding mode is realised, an infinitely high switching frequency is needed. Whenever the switching frequency is limited, an ideal sliding motion cannot take place and the trajectory will repeatedly cross the switching function [41], [48]. This effect is called chattering.

Chattering is a very real problem in the practical implementation of a sliding mode current controller. There are various methods to limit this chattering effect. The two methods that are going to be discussed in this section are the continuation approach and the tuning of the reaching law approach [41].

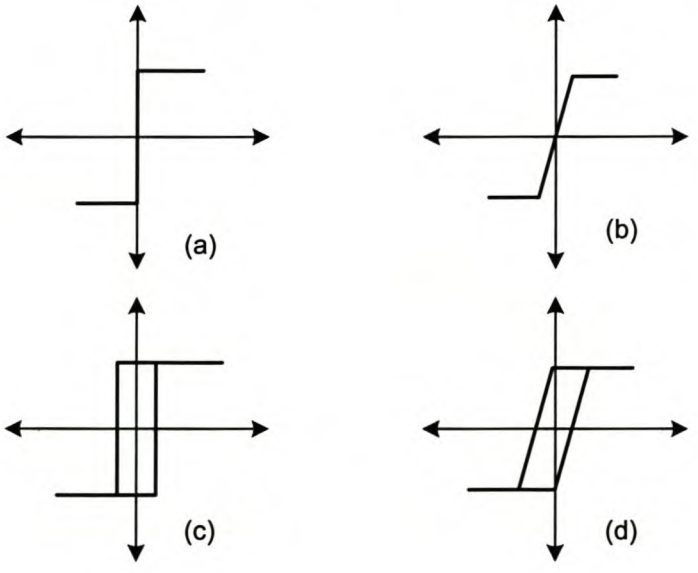


Figure 4-7 Continuous-approach switching functions

Lets consider the continuation approach first.

Many variable structure controllers currently use a control, which consists of a term that has a relay-like characteristic. The ideal relay-like characteristic shown in Figure 4-7 (a) is very difficult to realise practically. An alternative to the ideal relay-type control is the ideal saturating, continuous approximation shown in Figure 4-7 (b). This type of control introduces a boundary layer around the switching surface. By defining a boundary layer around the sliding function, the ideal sliding function is replaced by a pseudo sliding function [H9]. When inside this boundary layer, the control is chosen to be a continuous

approximation of the switching function. It can also be seen as a high-gain controller that is used near the switching surface. It must be noted that invariance is lost, but the controller still possesses robustness properties that are dependent on the boundary layer width. The second type of continuous controller is the hysteresis-type controller, namely the practical relay control, shown in Figure 4-7 (c), and the practical saturation control, shown in Figure 4-7 (d). The major disadvantage of the hysteresis-type controllers is their variable switching frequency. This is especially problematic in high-power applications.

The next section will discuss the ideal saturating continuous approach reaching mode controller in detail.

4.3.4.1 Ideal saturating current controller

Define the ideal saturating continuous approach reaching mode controller as:

$$u_{s-d} = \begin{cases} \text{sgn}(\sigma_d) & \text{for } \|\sigma_d\| \geq \delta \\ \frac{2}{\delta}\sigma_d & \|\sigma_d\| < \delta \end{cases} \tag{4-17}$$

$$u_{s-q} = \begin{cases} \text{sgn}(\sigma_q) & \text{for } \|\sigma_q\| \geq \delta \\ \frac{2}{\delta}\sigma_q & \|\sigma_q\| < \delta \end{cases} \tag{4-18}$$

$$u_{s-0} = \begin{cases} \text{sgn}(\sigma_0) & \text{for } \|\sigma_0\| \geq \delta \\ \frac{2}{\delta}\sigma_0 & \|\sigma_0\| < \delta \end{cases} \tag{4-19}$$

By combining the reaching mode controller with the equivalent controller, a control law can be determined that will adequately control the current-controlled voltage source inverter.

Simulation results for the proposed controller are given in Figure 4-8 and Figure 4-9.

4.3.4.2 Tuning of reaching law approach

This approach deals directly with the dynamics of the reaching mode. The reaching law is a differential equation that specifies the dynamics of the switching function $\sigma(x)$. By selecting appropriate parameters for the differential equation the dynamic quality of the current-controlled voltage source inverter can be controlled. A practical general form of the reaching law can be found from [48] as shown:

$$\dot{\boldsymbol{\sigma}} = -\mathbf{Q}\text{sgn}(\boldsymbol{\sigma}) - \mathbf{M}\text{h}(\boldsymbol{\sigma}) \tag{4-20}$$

where:

$\mathbf{Q} = diag(Q_d, Q_q, Q_0)$

$\mathbf{M} = diag(M_d, M_q, M_0)$

It must be noted that for the tuning of the reaching law approach, the gains k_1, k_2 of the switching function as given by Equation (4-10) are set to 1.

Two practical cases can be derived from Equation (4-20), namely the constant rate reaching method, and the constant plus proportional rate reaching method [48]. These two methods will be discussed in the rest of this section.

The constant rate reaching method can be defined as:

$$\dot{\boldsymbol{\sigma}} = -\mathbf{Q}\,\mathrm{sgn}(\boldsymbol{\sigma}) \tag{4-21}$$

This law forces the switching variables to reach the switching function at a constant rate of $|\dot{\sigma}_i| = -q_i$. This switching law is relatively simple to implement, but a drawback of this technique is that when q_i is too small, the reaching time will be too slow and when q_i is too large severe chattering will result.

Simulation results for the constant rate reaching method controller are given in Figure 4-10 and Figure 4-11.

The next practical case of the reaching law that is going to be discussed is the constant plus proportional rate reaching method:

$$\dot{\boldsymbol{\sigma}} = -\mathbf{Q}\,\mathrm{sgn}(\boldsymbol{\sigma}) - \mathbf{M}\boldsymbol{\sigma} \tag{4-22}$$

By adding the term $-\mathbf{M}\boldsymbol{\sigma}$ the state is forced faster to the switching function when $\boldsymbol{\sigma}$ is large.

Simulation results for the constant plus proportional rate reaching method controller are given in Figure 4-12 and Figure 4-13.

By considering the general reaching law as shown in Equation (4-20) and assuming that matrix **K** is the identity matrix, the control law can be determined as shown:

$$\dot{\boldsymbol{\sigma}} = \dot{\mathbf{x}}^* - \dot{\mathbf{x}} = -\mathbf{Q}\,\mathrm{sgn}(\boldsymbol{\sigma}) - \mathbf{M}\mathbf{h}(\boldsymbol{\sigma}) \tag{4-23}$$

$$\dot{\mathbf{x}}^* - (\mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} + \mathbf{G}) = -\mathbf{Q}\,\mathrm{sgn}(\boldsymbol{\sigma}) - \mathbf{M}\mathbf{h}(\boldsymbol{\sigma}) \tag{4-24}$$

$$\mathbf{u} = \{\mathbf{B}\}^{-1}\left\{\mathbf{Q}\,\mathrm{sgn}(\boldsymbol{\sigma}) + \mathbf{M}\mathbf{h}(\boldsymbol{\sigma}) + \mathbf{A}\mathbf{x} + \mathbf{G} + \dot{\mathbf{x}}^*\right\} \tag{4-25}$$

The control law can now be calculated for the different reaching law methods discussed:

The control law using the constant rate reaching method can be determined as shown:

$$\mathbf{u} = \{\mathbf{B}\}^{-1}\left\{\mathbf{Q}\,\mathrm{sgn}(\boldsymbol{\sigma}) + \mathbf{A}\mathbf{x} + \mathbf{G} + \dot{\mathbf{x}}^*\right\} \tag{4-26}$$

$$u_d = \underbrace{\frac{\left(r_l x_1 + V_d + L\dot{x}_1^*\right)}{V_{dc}}}_{u_{eq-d}} + \underbrace{Q_d\,\mathrm{sgn}(\sigma_d)}_{u_{s-d}} \tag{4-27}$$

$$u_q = \underbrace{\frac{\left(r_l x_2 + V_q + L\dot{x}_2^*\right)}{V_{dc}}}_{u_{eq-q}} + \underbrace{Q_q\,\mathrm{sgn}(\sigma_q)}_{u_{s-q}} \tag{4-28}$$

$$u_0 = \underbrace{\frac{\left(0.25r_l + 0.75r_N\right)x_3 + V_0 + \left(0.25L + 0.75L_N\right)\dot{x}_3^*}{V_{dc}}}_{u_{eq-0}} + \underbrace{Q_0\,\mathrm{sgn}(\sigma_0)}_{u_{s-0}} \tag{4-29}$$

and the control law for the constant plus proportional rate reaching method be determined as shown:

$$\mathbf{u} = \{\mathbf{B}\}^{-1}\left\{\mathbf{Q}\,\mathrm{sgn}(\boldsymbol{\sigma}) + \mathbf{M}\boldsymbol{\sigma} + \mathbf{A}\mathbf{x} + \mathbf{G} + \dot{\mathbf{x}}^{*}\right\} \tag{4-30}$$

$$u_d = \underbrace{\frac{\left(r_l x_1 + V_d + L\dot{x}_1^{*}\right)}{V_{dc}}}_{u_{eq-d}} + \underbrace{Q_d\,\mathrm{sgn}(\sigma_d) + M_d\sigma_d}_{u_{s-d}} \tag{4-31}$$

$$u_q = \underbrace{\frac{\left(r_l x_2 + V_q + L\dot{x}_2^{*}\right)}{V_{dc}}}_{u_{eq-q}} + \underbrace{Q_q\,\mathrm{sgn}(\sigma_q) + M_q\sigma_q}_{u_{s-q}} \tag{4-32}$$

$$u_0 = \underbrace{\frac{\left(0.25r_l + 0.75r_N\right)x_3 + V_0 + \left(0.25L + 0.75L_N\right)\dot{x}_3^{*}}{V_{dc}}}_{u_{eq-0}} + \underbrace{Q_0\,\mathrm{sgn}(\sigma_0) + M_0\sigma_0}_{u_{s-0}} \tag{4-33}$$

The next section will show simulation results using Simplorer® version 4.2 for the sliding mode current controllers discussed.

4.3.5 Simulation results

The simulation results seen in Figure 4-8 to Figure 4-13 are the results from the simulation setup as shown in Appendix C1. In order to evaluate only the performance of the sliding mode current controllers the time delay and dead time are set to 0 in the simulations. The reference current components are the same as the reference current components that were used to evaluate the performance of the predictive current controller.

Figure 4-8 and Figure 4-9 show respectively the reference currents (black traces) and the actual currents (coloured traces) regulated by the inverter with and without the neutral inductor being connected for the ideal saturating controller.

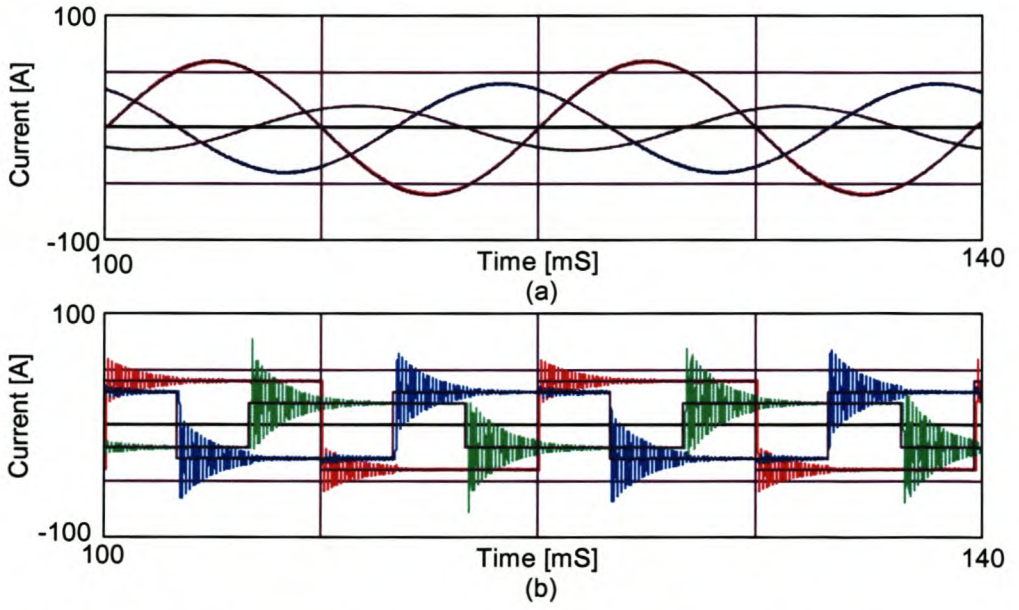


Figure 4-8 Sliding mode controller – ideal saturating controller with neutral inductor not connected

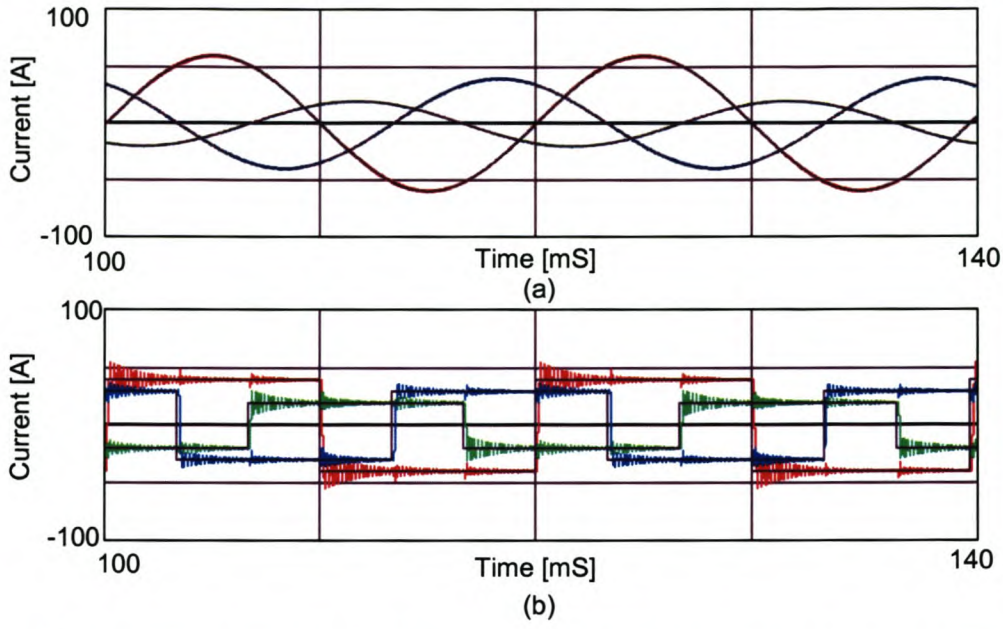


Figure 4-9 Sliding mode controller – ideal saturating controller with neutral inductor connected

The gains used for the ideal saturation current controller in this simulation are shown in Table 11.

Table 11 Ideal saturating controller parameters

Neutral inductor not connected	Neutral inductor connected
k1 =0.015	k1 =0.015
k2 =0.00375	k1 =0.015

In Figure 4-8 (b) a large overshoot can be seen when a sudden step change is applied to the reference current signal. In Figure 4-9 (b) the overshoot is dampened due to the extra neutral inductor being connected. For the low-frequency reference current signals, this current controller work satisfactorily.

Figure 4-10 and Figure 4-11 show respectively the reference currents (black traces) and the actual currents (coloured traces) regulated by the inverter with and without the neutral inductor being connected for the constant rate controller.

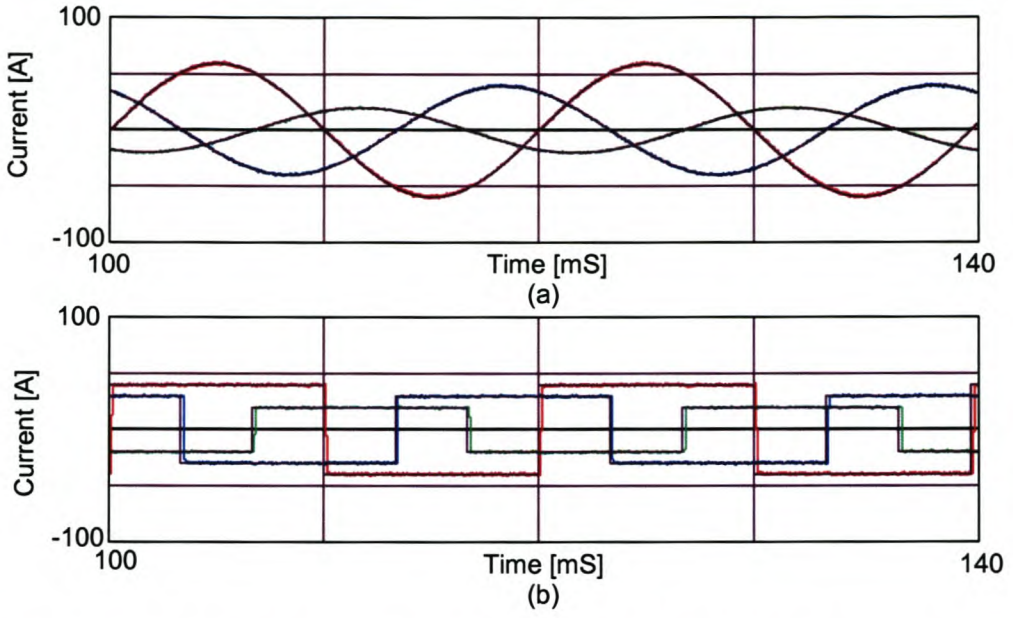


Figure 4-10 Sliding mode controller – Constant rate controller with neutral inductor not connected

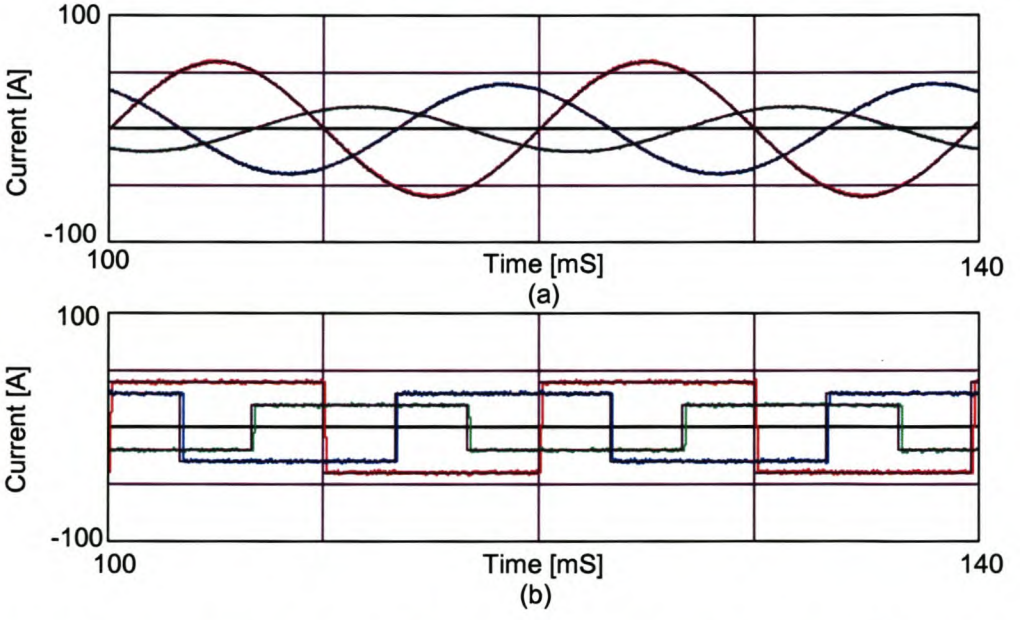


Figure 4-11 Sliding mode controller – Constant rate controller with neutral inductor connected

The gains used for the constant rate current controller in this simulation are shown in Table 12.

Table 12 Constant rate controller parameters

Neutral inductor not connected	Neutral inductor connected
$Q_d = 0.01$	$Q_d = 0.01$
$Q_q = 0.01$	$Q_q = 0.01$
$Q_0 = 0.0025$	$Q_0 = 0.01$

Figure 4-10 and Figure 4-11 show that the constant rate current controller works satisfactorily even for sudden step changes in the reference current signals.

Figure 4-12 and Figure 4-13 show respectively the reference currents (black traces) and the actual currents (coloured traces) regulated by the inverter with and without the neutral inductor being connected for the constant rate + proportional controller.

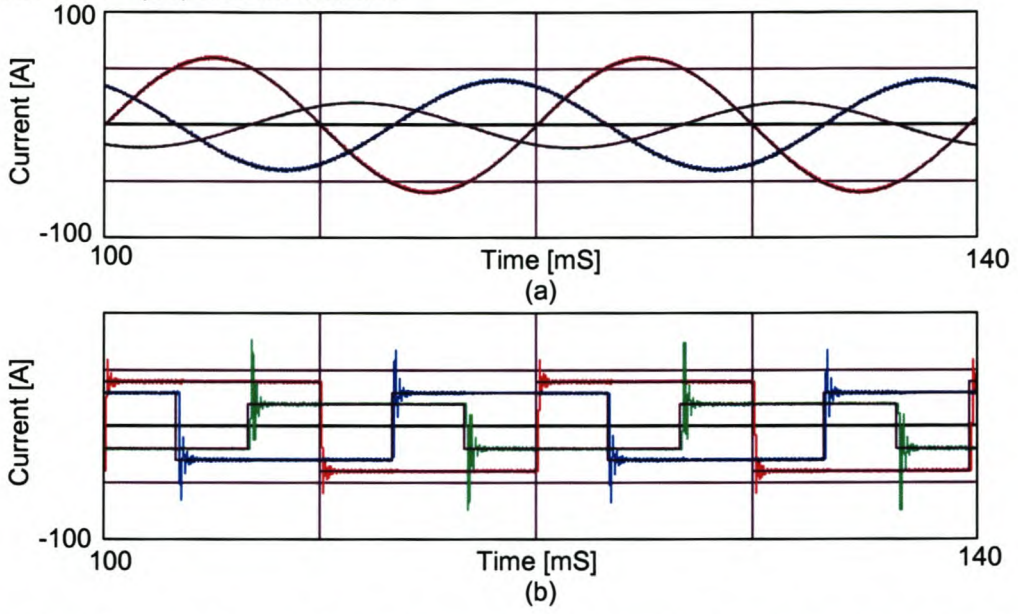


Figure 4-12 Sliding mode controller – Constant rate + proportional controller with neutral inductor not connected

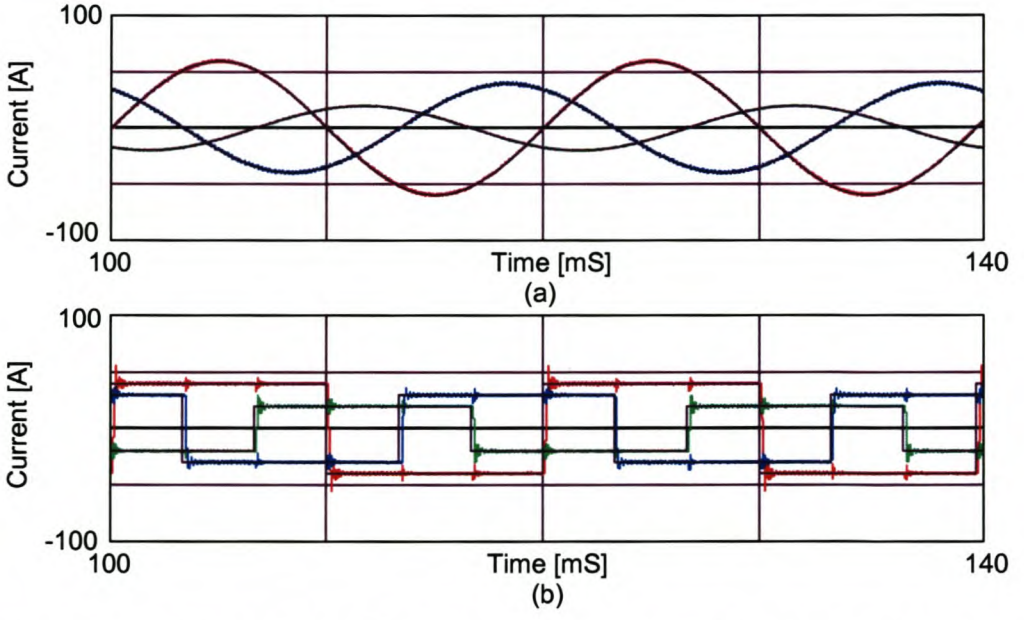


Figure 4-13 Sliding mode controller – Constant rate + proportional controller with neutral inductor connected

The gains used for the constant rate current controller in this simulation are shown in Table 13.

Table 13 Constant rate + proportional controller parameters

Neutral inductor not connected	Neutral inductor connected
$Q_d = 0.003$	$Q_d = 0.003$
$Q_q = 0.003$	$Q_q = 0.003$
$Q_0 = 0.00075$	$Q_0 = 0.003$
$M_d = 0.016$	$M_d = 0.016$
$M_q = 0.016$	$M_q = 0.016$
$M_0 = 0.004$	$M_0 = 0.016$

In Figure 4-12 (b) a large overshoot can be seen when a sudden step change is applied to the reference current signal. In Figure 4-13 (b) the overshoot is dampen due to the extra neutral inductor being connected. For the low frequency reference current signals this current controller work satisfactorily.

4.3.6 Summary

Two categories of reference signal-tracking algorithms were investigated, namely predictive current controllers and sliding mode controllers. The detailed design process for these current controllers was provided, and simulation results illustrated that the proposed current controllers work satisfactorily.

Chapter 5 will discuss the practical implications when the discussed current controllers are implemented practically.

5. Practical considerations

5.1 Introduction

By considering ideal effects the current controllers work satisfactorily; but the practical implementation of these controllers introduce factors that contribute to the deterioration of the voltage source inverter's ability to achieve proper reference current tracking.

This chapter will address some of the practical implications of the current-controlled voltage source inverter.

In Section 5.2 a proper compensating technique will be proposed to compensate for the effect that sampling and computational time delay have on the performance of the system. This will be followed by investigating the effect that dead-time has on the system, and based on this discussion a dead-time compensating strategy will be proposed.

In Section 5.4 and Section 5.5 a detailed analysis will be done through simulation on the proposed current regulators, taking practical issues into consideration. Two sets of current references will be applied to test the performance. Sinusoidal references will be applied to test the tracking performance of the controller when the rate of current change is relatively small, and square waveforms will be applied to investigate the performance of the controller when the rate of current change is high (step response). The simulation models used in these two sections is described in Appendix C-1, and the reference current components used are the same as in Chapter 4. The actual current waveforms in Section 5.2 to Section 5.5 is labelled in the following manner; phase A current-red, phase B current-blue, and phase C current-green.

Finally the shunt active power filter performance will be investigated through simulation by applying the discussed theories.

5.2 Time delay incorporated

The time it takes to sample the current and voltage values and the time that the DSP takes to process the sampled values leads to a T_s time delay between sampling and actually applying the duty cycles to the inverter.

A strategy will be proposed to compensate for this effect by predicting the current value 1 sampling period T_s ahead by using the dynamic model of the system. It must be noted that the proposed prediction method assumes that the DC-bus voltage and the EMF voltage are constant during a sample period. In order to discuss the time delay compensation method, consider the dynamic model as given in Equation (4-1).

The differential term in Equation (4-1) can be approximated using the forward rectangular version of Euler's method [H5] as shown:

$$\frac{d}{dt}I_x = \frac{I_x(k+1) - I_x(k)}{T_s} \tag{5-1}$$

where

x represents the d, q and 0 components

$I_x(k+1)$ is the predicted current

$I_x(k)$ is the sampled value

From Equation (4-1) and Equation (5-1) the following three equations can be obtained:

$$\frac{I_d(k+1) - I_d(k)}{T_s} = -\frac{r_l}{L}I_d(k) + \frac{V_{dc}(k)}{L}u_d - \frac{V_d(k)}{L} \tag{5-2}$$

$$\frac{I_q(k+1) - I_q(k)}{T_s} = -\frac{r_l}{L}I_q(k) + \frac{V_{dc}(k)}{L}u_q - \frac{V_q(k)}{L} \tag{5-3}$$

$$\frac{I_0(k+1) - I_0(k)}{T_s} = -\frac{(0.25r_l + 0.75r_N)}{(0.25L + 0.75L_N)}I_0(k) + \frac{V_{dc}(k)}{(0.25L + 0.75L_N)}u_0 - \frac{V_0(k)}{(0.25L + 0.75L_N)} \tag{5-4}$$

By rearranging the above equations the future value can be determined as shown:

$$I_d(k+1) = \left(1 - \frac{T_s r_l}{L}\right)I_d(k) + \frac{T_s V_{dc}(k)}{L}u_d - \frac{T_s V_d(k)}{L} \tag{5-5}$$

$$I_q(k+1) = \left(1 - \frac{T_s r_l}{L}\right)I_q(k) + \frac{T_s V_{dc}(k)}{L}u_q - \frac{T_s V_q(k)}{L} \tag{5-6}$$

$$I_0(k+1) = \left(1 - \frac{T_s(0.25r_l + 0.75r_N)}{(0.25L + 0.75L_N)}\right)I_0(k) + \frac{T_s V_{dc}(k)}{(0.25L + 0.75L_N)}u_0 - \frac{T_s V_0(k)}{(0.25L + 0.75L_N)} \tag{5-7}$$

It must be noted that the duty cycles u_d, u_q and u_0 are the actual quantities sent to the inverter, thus when the reference voltage vector, $\mathbf{u}_{ref}$, is limited, the limited reference vector, $\mathbf{u}_{refl}$, must be used.

The effect that the time delay has on the performance of the system will now be discussed through simulation results. The simulation model used in the rest of this section is described in Appendix C1, and the reference current components are the same as in Chapter 4.

In Figure 5-1 (a), Figure 5-2 (a), Figure 5-3 (a) and Figure 5-4 (a) the reference current (black traces) and the actual phase currents (Phase A-red, Phase B-blue, Phase C-green) are shown when the predictive current controller, as was discussed in Chapter 4, is implemented in a practical system without any compensation for practical effects. By a practical system is meant that the effect of time delay and dead-time is included in the simulation model.

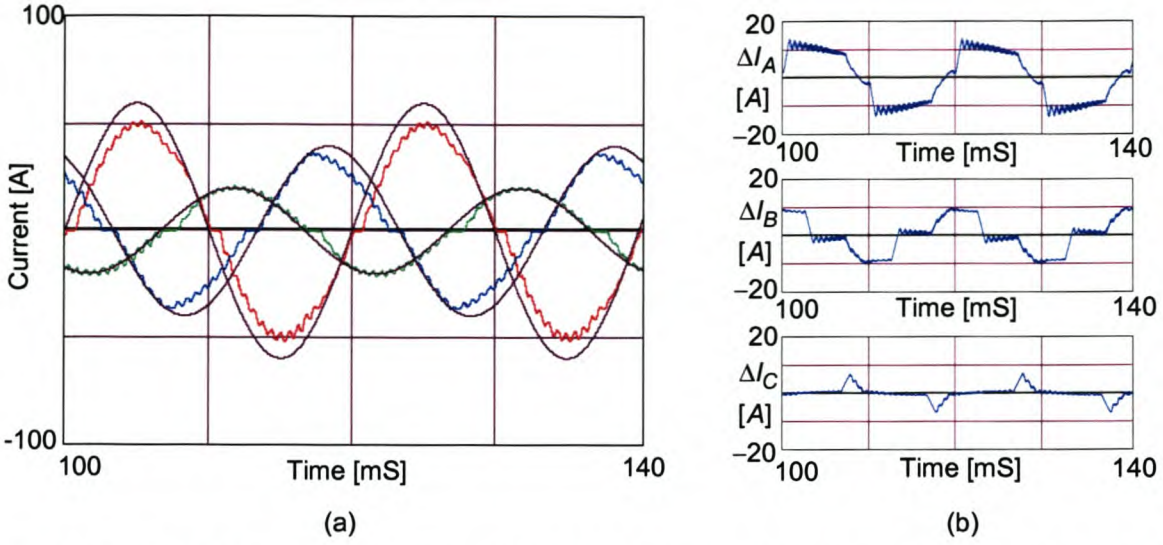


Figure 5-1 Predictive current controller without neutral inductor connected, using sinusoidal references, with no prediction implemented.

Figure 5-1 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 8.9 A, 6.1 A and 2.1 A respectively.

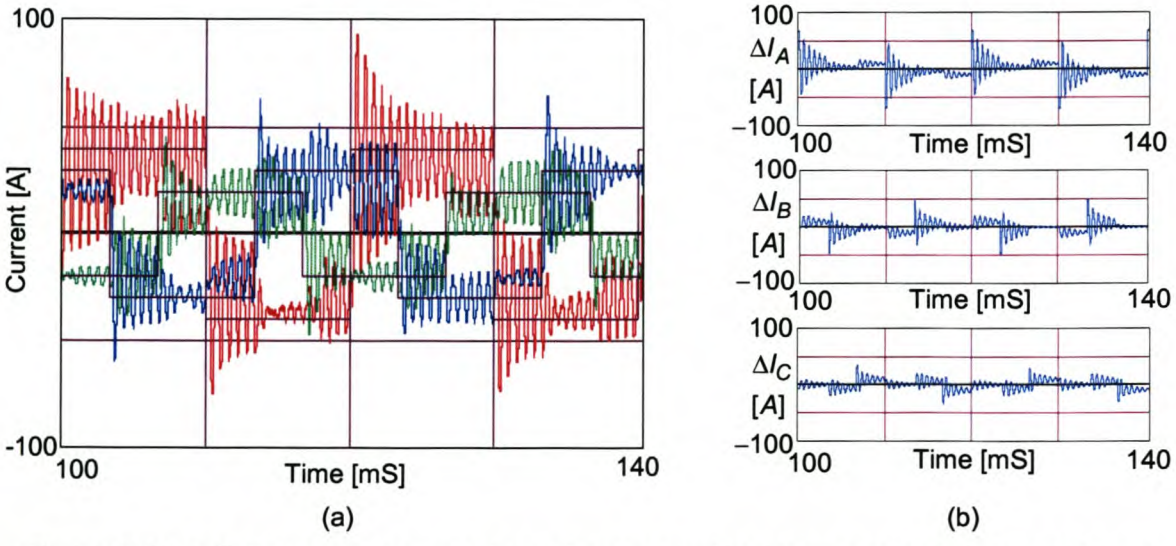


Figure 5-2 Predictive current controller without neutral inductor connected, using square references, with no time delay compensation implemented.

Figure 5-2 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 17.0 A, 11.8 A and 9.8 A respectively.

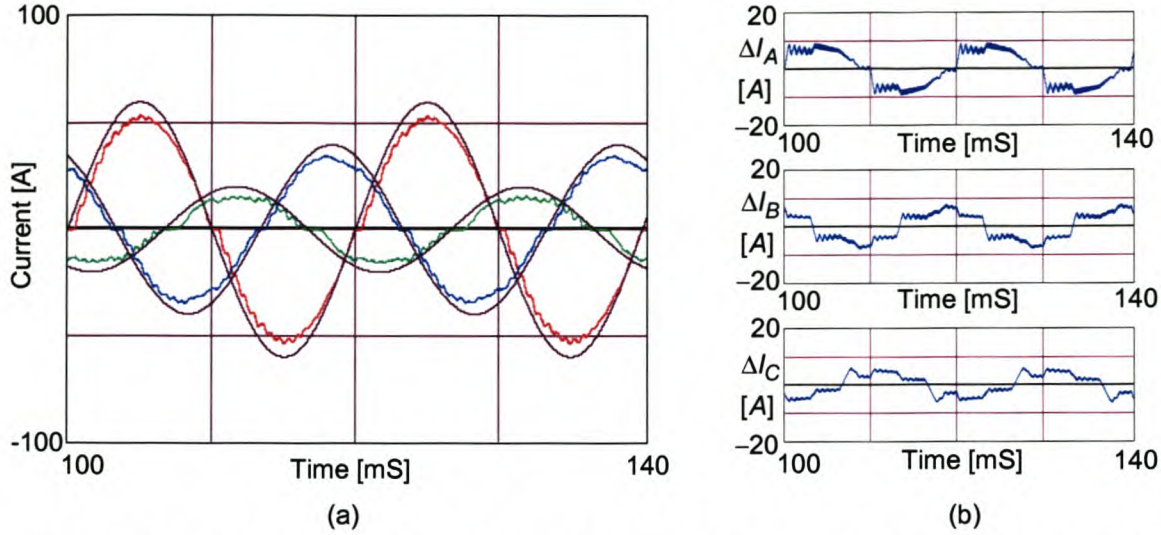


Figure 5-3 Predictive current controller with neutral inductor connected, using sinusoidal references, with no time delay compensation implemented.

Figure 5-3 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 6.0 A, 4.6 A and 3.7 A respectively.

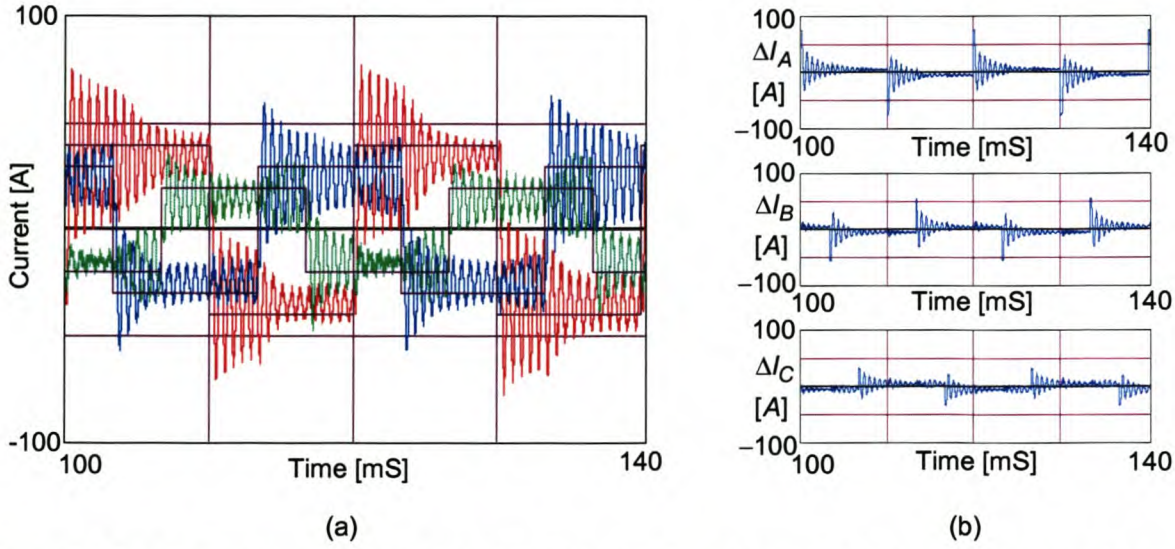


Figure 5-4 Predictive current controller with neutral inductor connected, using square references, with no time delay compensation implemented.

Figure 5-4 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 14.0 A, 11.8 A and 8.6 A respectively.

As can be seen from the above simulations, when a step is applied to the reference current signal, oscillations results. This can be attributed to the one sampling time delay between the measured current and the application of the control signal. This is best illustrated with the aid of Figure 5-5. At $t = 0$ the actual current is sampled and the control vector, $\mathbf{u}_{ref}(1)$, is calculated to force the actual current towards the reference current, but there is one sampling time delay between the sampled actual current value and

applying the control vector. At $t = 1T_s$, when $\mathbf{u}_{ref}(1)$ is applied to the inverter, the actual current is measured and a new control vector, $\mathbf{u}_{ref}(2)$, is calculated. The control vector ,$\mathbf{u}_{ref}(2)$, however, is only applied at $t = 2T_s$ in order to force the actual current to be equal to the reference current signal at $t = 3T_s$. At $t = 2T_s$ the actual current is sampled and a new control vector, $\mathbf{u}_{ref}(3)$, is calculated that will be applied at $t = 3T_s$. At $t = 3T_s$ the actual current value is equal to the reference vector, but the control vector that is going to be applied to the inverter at $t = 3T_s$ was calculated when the actual current value was 0. This results in overshoot. The oscillations decay due to the dead-time effects.

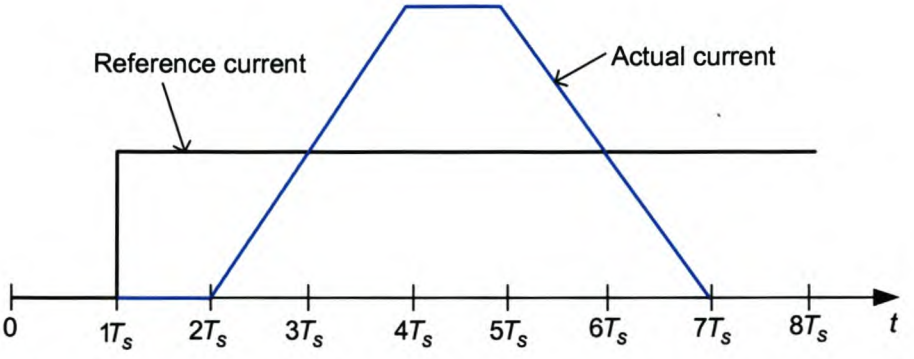
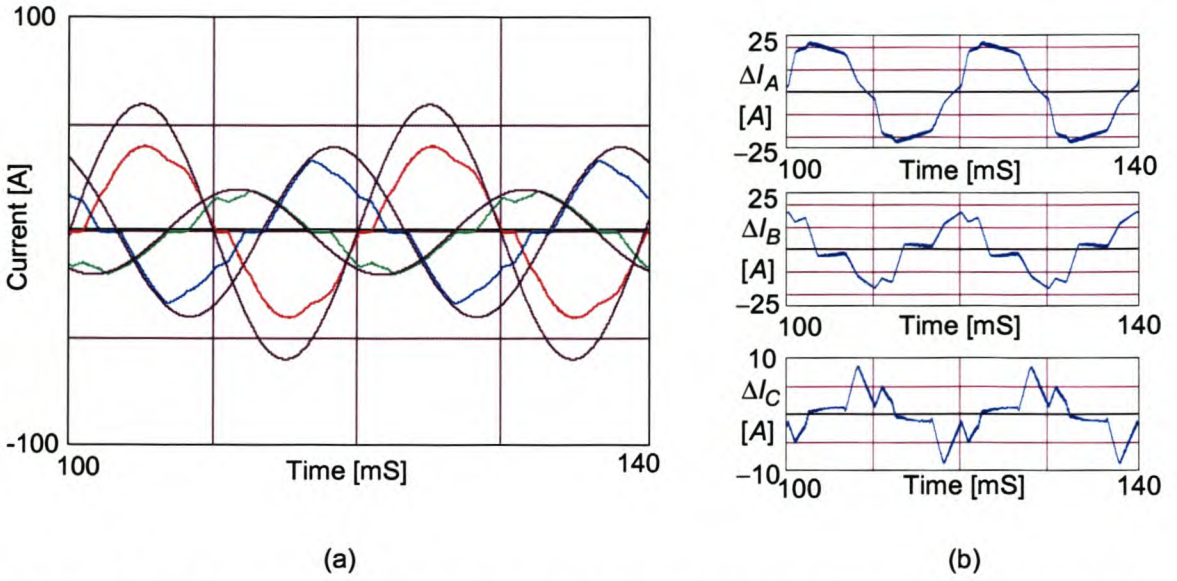


Figure 5-5 Explanation of the oscillations when the time delay compensation is not implemented

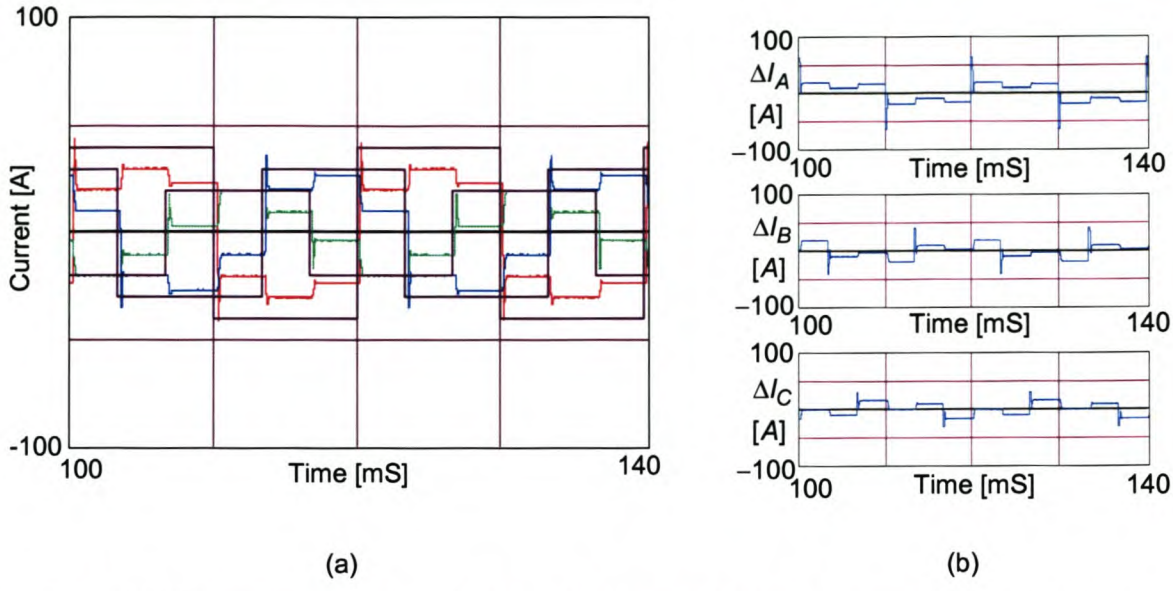
In Figure 5-6 (a), Figure 5-7 (a), Figure 5-8 (a) and Figure 5-9 (a) the reference current (black traces) and the actual current (blue, red, green traces) are shown when the predictive current controller, is implemented in a practical system with the discussed time-delay compensation technique implemented.



(a) (b)

Figure 5-6 Predictive current controller without neutral inductor connected, using sinusoidal references, with time delay compensation implemented.

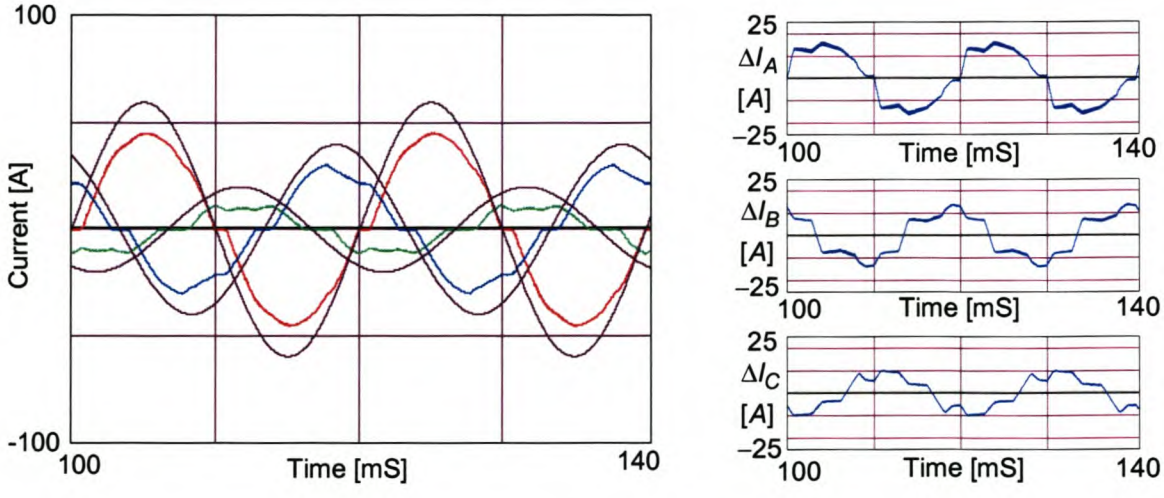
Figure 5-6 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 16.0 A, 9.9 A and 3.6 A respectively.



(a) (b)

Figure 5-7 Predictive current controller without neutral inductor connected, using square references, with time delay compensation implemented.

Figure 5-7 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 17.7 A, 13.1 A and 11.5 A respectively.



(a) (b)

Figure 5-8 Predictive current controller with neutral inductor connected, using sinusoidal references, with time delay compensation implemented.

Figure 5-8 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 11.3 A, 8.8 A and 6.6 A respectively.

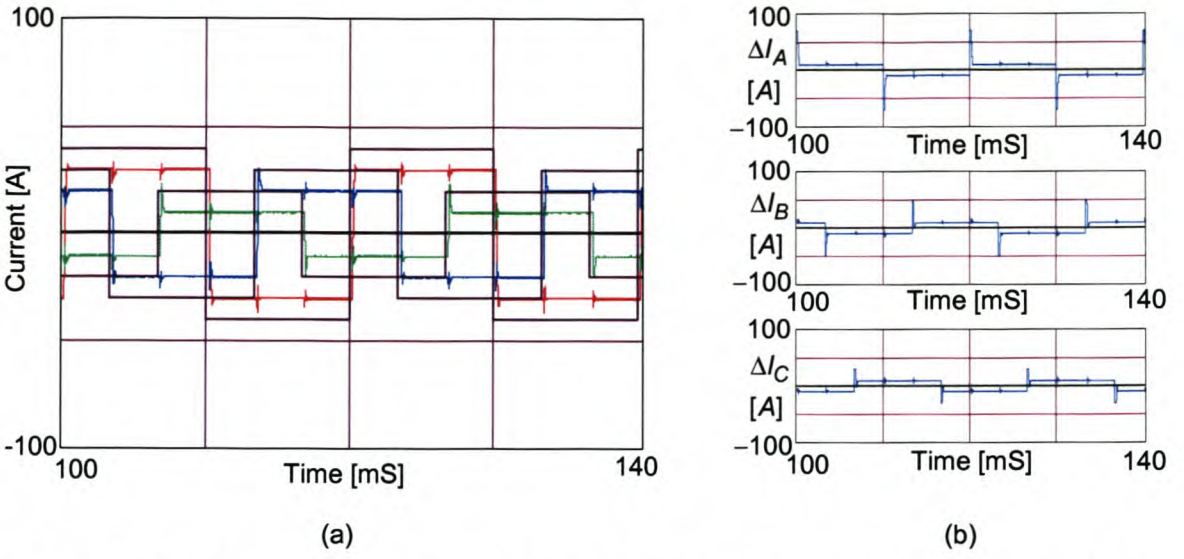


Figure 5-9 Predictive current controller with neutral inductor connected, using square references, with time delay compensation implemented.

Figure 5-9 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 13.9 A, 12.0 A and 10.3 A respectively.

As can be seen from the above figures, when the time delay compensator is implemented the oscillations disappear, but the rms current error values increase. This is due to dead-time effects and the absence of the oscillations that were indirectly over compensating, thus reducing the rms current error.

The next section will discuss the effect that dead-time has on the performance of a current-controlled voltage source inverter.

5.3 Dead-time compensation techniques

Another factor that has a detrimental effect on the performance of a current-controlled voltage source inverter is dead time.

Dead time is the short time that elapses between switching one device in an inverter leg off and the other device in the inverter leg on in order to prevent a leg short-circuit.

Oh *et al.* in [35] proposed a dead-time compensation technique for three-phase three-wire current controlled inverters using the space vector method. Their compensating method is based on considering the direction of the currents. They, however, did not address in [35] the effect of the current changing direction during a switching cycle.

The theory proposed in [35] will be extended to devise a dead-time compensation technique for current controlled three-phase four-wire voltage source inverters. Additionally the issue of a current direction change during a switching cycle will be addressed.

Sections 5.3.1, 5.3.2 and 5.3.3 discuss the extension to the dead-time compensation technique proposed by [35] when the currents' direction does not change during a switching cycle. This development will be done in three parts. The first part investigates the effect that dead time has on one phase arm of the

inverter, as was discussed by [35]. This will be followed by an analysis of the three-phase four-wire inverter in mode 1, and finally the three-phase four-wire inverter will be analysed in mode 2. Oh *et al.* in [35] defined a mode 1 when the duration of the driving pulse in the inverter is longer than the dead time, and a mode 2 when the duration of the driving pulse in the inverter is shorter than the dead time.

Section 5.3.4 discuss the effects of dead-time compensation when the current direction change during a switching cycle, and a technique will be proposed that will take this effect into consideration.

The indices for the three-phase four-leg inverter shown in Figure 5-10 will be used to aid the discussion.

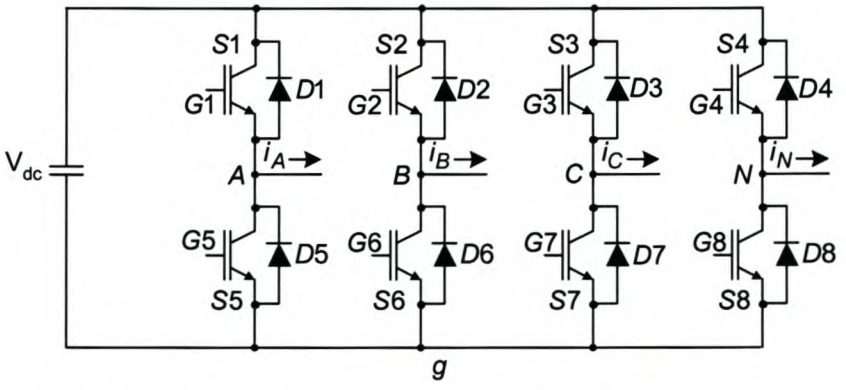


Figure 5-10 Three-phase 4-leg inverter used to aid in the discussion

5.3.1 Analysis of one phase arm

In order to investigate the influence that dead-time and switching times have on voltage waveforms the behavior of one phase leg is investigated:

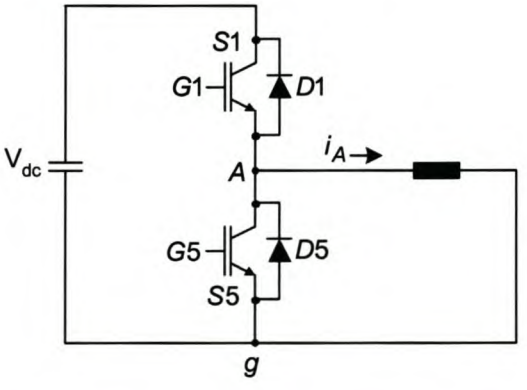


Figure 5-11 One-leg of the three-phase four-leg inverter

During dead-time the inverter output voltages depend only on the current direction. By considering Figure 5-11 the following can be seen. During dead-time when $i_A > 0$ the diode $D5$ will be conducting and thus the output voltage will only be dependent on the switching action of $S1$. Alternately, when $i_A < 0$ the diode $D1$ will be conducting and the output voltage will only be dependent on the switching action of $S5$.

The effect that dead-time has on the output voltage of a one-leg inverter is illustrated graphically in Figure 5-12.

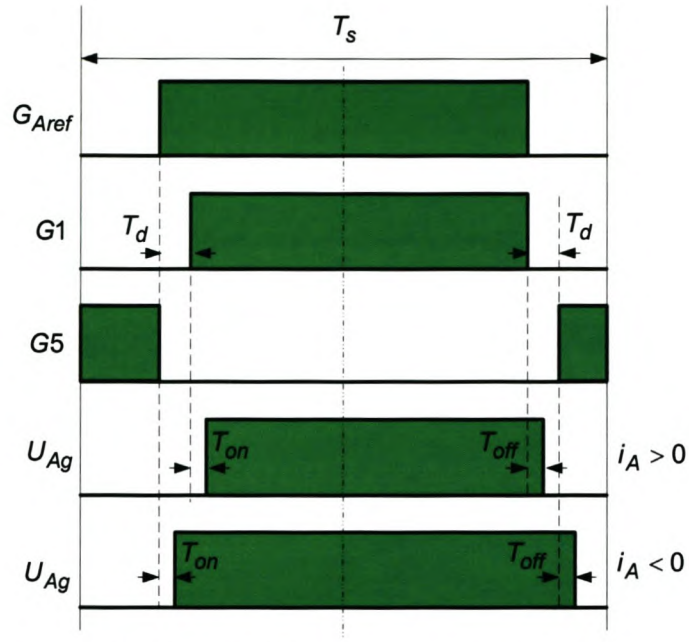


Figure 5-12 Effect of dead-time on one-leg of inverter

From Figure 5-12 it can be seen that when $i_A > 0$ the actual switching pulse, U_{Ag}, is narrower than the reference pulse, G_{Aref}, and when $i_A < 0$ the actual switching pulse is wider than the reference pulse, G_{Aref}. This can be illustrated mathematically as [35]:

$$T_{aon} = T_{aref} - \{(T_d + T_{on}) - T_{off}\} \quad \text{for} \quad i_A > 0 \tag{5-8}$$

$$T_{aon} = T_{aref} + \{(T_d + T_{on}) - T_{off}\} \quad \text{for} \quad i_A < 0 \tag{5-9}$$

where T_{aon} is the actual switching time

T_{aref} is the reference switching time

T_{on} and T_{off} are the turn-on and turn-off times of the switching devices

T_d is the dead-time

From Equation (5-8) and (5-9) a general equation can be determined for the respective legs of the inverter [35]:

$$T_{pon} = T_{pref} - \text{sgn}(i_p) T_e \tag{5-10}$$

where $p = A,B,C,N$

$$T_e = (T_d + T_{on}) - T_{off}$$

$$\text{sgn}(i_p) = \begin{cases} 1 & \text{for } i_p > 0 \\ -1 & \text{for } i_p < 0 \end{cases}$$

It must also be noted that the respective average phase to ground (g) voltages can be determined as:

$$U_{pg} = V_{dc}\left(\frac{T_{pon}}{T_s}\right) \quad \text{for } p = A,B,C,N \tag{5-11}$$

This provides the basis for investigating the effect that dead-time has on three-phase four-wire inverters.

5.3.2 Four-leg inverter analysis on dead-time (mode 1)

The effect that dead-time and switching times have on the phase-to-phase voltages when in mode 1 is illustrated graphically in Figure 5-13.

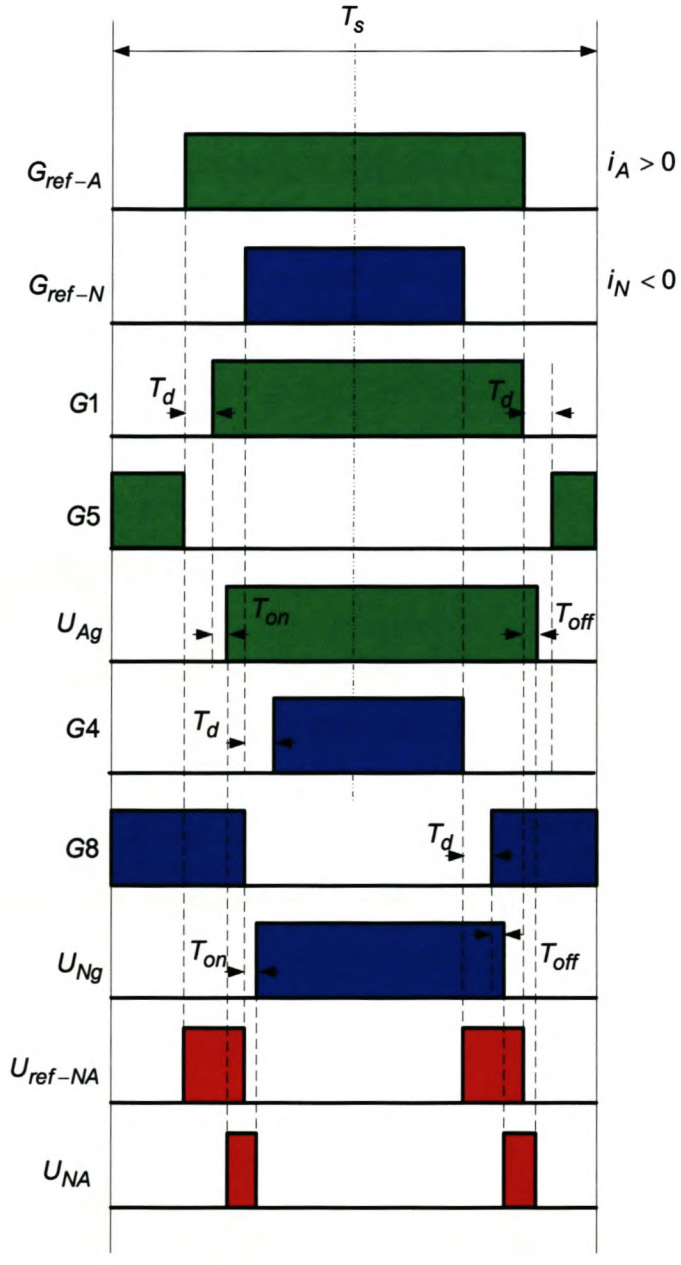


Figure 5-13 – Effect of dead-time on the phase-to-phase voltages when in mode 1

To determine the compensating times it must be noted that the current vectors in a three-phase four-leg inverter add together as shown:

$$i_A + i_B + i_C + i_N = 0 \tag{5-12}$$

From the above equation it can be seen that the phase currents can have two possible combinations: only one phase current direction is different from the others, or two of the phase currents are in the same direction and the other two phase currents are in the opposite direction.

By considering the average phase-to-phase voltages, the effect that dead-time has on the two possible combinations can be investigated.

Three of the combinations' phase-to-phase voltages are summarised in Table 14 in order to illustrate that the actual inverter average phase-to-phase voltages are different from the expected values.

Table 14 Three combinations in mode 1

(a) $i_A > 0, i_B > 0, i_C > 0, i_N < 0$	$U_{Ag} = V_{dc}\left(\frac{T_{aref} - T_e}{T_s}\right)$ $U_{Bg} = V_{dc}\left(\frac{T_{bref} - T_e}{T_s}\right)$ $U_{Cg} = V_{dc}\left(\frac{T_{cref} - T_e}{T_s}\right)$ $U_{Ng} = V_{dc}\left(\frac{T_{Nref} + T_e}{T_s}\right)$	$U_{AN} = U_{Ag} - U_{Ng} = V_{dc}\left(\frac{T_{aref} - T_{Nref} - 2T_e}{T_s}\right)$ $U_{BN} = U_{Bg} - U_{Ng} = V_{dc}\left(\frac{T_{bref} - T_{Nref} - 2T_e}{T_s}\right)$ $U_{CN} = U_{Cg} - U_{Ng} = V_{dc}\left(\frac{T_{cref} - T_{Nref} - 2T_e}{T_s}\right)$ $U_{AB} = U_{Ag} - U_{Bg} = V_{dc}\left(\frac{T_{aref} - T_{bref}}{T_s}\right)$ $U_{BC} = U_{Bg} - U_{Cg} = V_{dc}\left(\frac{T_{bref} - T_{cref}}{T_s}\right)$ $U_{CA} = U_{Cg} - U_{Ag} = V_{dc}\left(\frac{T_{cref} - T_{aref}}{T_s}\right)$
(b) $i_A < 0, i_B < 0, i_C < 0, i_N > 0$	$U_{Ag} = V_{dc}\left(\frac{T_{aref} + T_e}{T_s}\right)$ $U_{Bg} = V_{dc}\left(\frac{T_{bref} + T_e}{T_s}\right)$ $U_{Cg} = V_{dc}\left(\frac{T_{cref} + T_e}{T_s}\right)$ $U_{Ng} = V_{dc}\left(\frac{T_{Nref} - T_e}{T_s}\right)$	$U_{AN} = U_{Ag} - U_{Ng} = V_{dc}\left(\frac{T_{aref} - T_{Nref} + 2T_e}{T_s}\right)$ $U_{BN} = U_{Bg} - U_{Ng} = V_{dc}\left(\frac{T_{bref} - T_{Nref} + 2T_e}{T_s}\right)$ $U_{CN} = U_{Cg} - U_{Ng} = V_{dc}\left(\frac{T_{cref} - T_{Nref} + 2T_e}{T_s}\right)$ $U_{AB} = U_{Ag} - U_{Bg} = V_{dc}\left(\frac{T_{aref} - T_{bref}}{T_s}\right)$ $U_{BC} = U_{Bg} - U_{Cg} = V_{dc}\left(\frac{T_{bref} - T_{cref}}{T_s}\right)$ $U_{CA} = U_{Cg} - U_{Ag} = V_{dc}\left(\frac{T_{cref} - T_{aref}}{T_s}\right)$

(c) $i_A < 0, i_B > 0, i_C < 0, i_N > 0$	$U_{Ag} = V_{dc}\left(\frac{T_{aref} + T_e}{T_s}\right)$ $U_{Bg} = V_{dc}\left(\frac{T_{bref} - T_e}{T_s}\right)$ $U_{Cg} = V_{dc}\left(\frac{T_{cref} + T_e}{T_s}\right)$ $U_{Ng} = V_{dc}\left(\frac{T_{Nref} - T_e}{T_s}\right)$	$U_{AN} = U_{Ag} - U_{Ng} = V_{dc}\left(\frac{T_{aref} - T_{Nref} + 2T_e}{T_s}\right)$ $U_{BN} = U_{Bg} - U_{Ng} = V_{dc}\left(\frac{T_{bref} - T_{Nref}}{T_s}\right)$ $U_{CN} = U_{Cg} - U_{Ng} = V_{dc}\left(\frac{T_{cref} - T_{Nref} + 2T_e}{T_s}\right)$ $U_{AB} = U_{Ag} - U_{Bg} = V_{dc}\left(\frac{T_{aref} - T_{bref} + 2T_e}{T_s}\right)$ $U_{BC} = U_{Bg} - U_{Cg} = V_{dc}\left(\frac{T_{bref} - T_{cref} - 2T_e}{T_s}\right)$ $U_{CA} = U_{Cg} - U_{Ag} = V_{dc}\left(\frac{T_{cref} - T_{aref}}{T_s}\right)$

From Table 14 it can be seen that the actual average phase-to-phase voltages are different from the expected phase-to-phase voltages. From Table 14 the amount by which the compensating times must be adjusted can be calculated in order to ensure that the inverter's phase-to-phase voltages are equal to the reference voltages. Table 15 shows the compensating time that is necessary to ensure that the actual voltages and the reference voltages are equal for the three combinations discussed in Table 14.

Table 15 – Compensating times for the three discussed combinations in mode 1

Combination	Compensating time
(a)	$T_{Ncom} = T_{Nref} - 2T_e$
(b)	$T_{Ncom} = T_{Nref} + 2T_e$
(c)	$T_{acom} = T_{aref} + 2T_e$ $T_{ccom} = T_{cref} + 2T_e$ or $T_{bcom} = T_{bref} + 2T_e$ $T_{Ncom} = T_{Nref} + 2T_e$

To ease the implementation of the dead-time compensating algorithm, Table 15 can be simplified to form general compensating times for mode 1 as shown:

$$T_{pcom} = \begin{cases} T_{pref} + T_e & \text{for } i_p > 0 \\ T_{pref} - T_e & \text{for } i_p < 0 \end{cases} \quad (5\text{-}13)$$

5.3.3 Four-leg inverter analysis on dead-time (mode 2)

The effect that dead-time and switching times have on the phase-to-phase voltages when in mode 2 is shown in Figure 5-14. Figure 5-14 (a) illustrates the effect of dead-time on the actual voltage when the narrow pulse current direction is larger than 0 and Figure 5-14 (b) illustrates the effect of dead-time on the actual voltage when the narrow pulse current direction is smaller than 0.

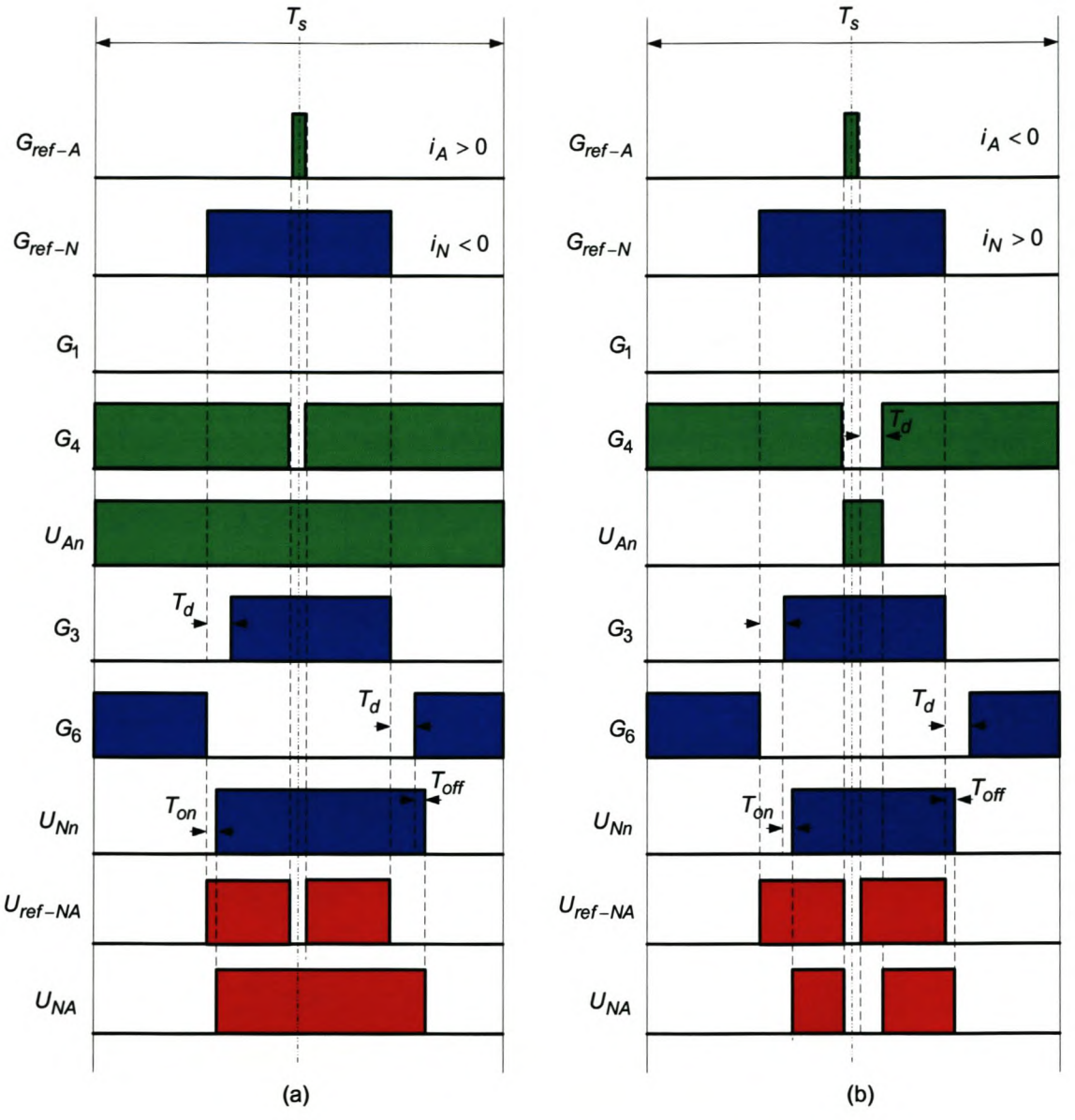


Figure 5-14 Effect of dead-time on the phase-to-phase voltages when in mode 2

Two combinations are illustrated in Table 16. The one combination illustrates the effect that dead-time has on the actual voltage waveform when the narrow pulse current direction is larger than 0, and the other combination is when the narrow pulse current direction is smaller than 0.

Table 16 Actual average phase-to-phase voltages for mode 2

i_A narrow, $i_A > 0$, $i_B > 0$, $i_C > 0$, $i_N < 0$	$U_{Ag} = 0$ $U_{Bg} = V_{dc}\left(\frac{T_{bref} - T_e}{T_s}\right)$ $U_{Cg} = V_{dc}\left(\frac{T_{cref} - T_e}{T_s}\right)$ $U_{Ng} = V_{dc}\left(\frac{T_{Nref} + T_e}{T_s}\right)$	$U_{AN} = U_{Ag} - U_{Ng} = V_{dc}\left(\frac{-T_{Nref} - T_e}{T_s}\right) = U_{ANref} - V_{dc}\left(\frac{T_{Aref} - T_e}{T_s}\right)$ $U_{BN} = U_{Bg} - U_{Ng} = V_{dc}\left(\frac{T_{bref} - T_{Nref} - 2T_e}{T_s}\right) = U_{BNref} - V_{dc}\left(\frac{2T_e}{T_s}\right)$ $U_{CN} = U_{Cg} - U_{Ng} = V_{dc}\left(\frac{T_{cref} - T_{Nref} - 2T_e}{T_s}\right) = U_{CNref} - V_{dc}\left(\frac{2T_e}{T_s}\right)$ $U_{AB} = U_{Ag} - U_{Bg} = V_{dc}\left(\frac{-T_{bref} + T_e}{T_s}\right) = U_{ABref} - V_{dc}\left(\frac{T_{Aref} - T_e}{T_s}\right)$ $U_{BC} = U_{Bg} - U_{Cg} = V_{dc}\left(\frac{T_{bref} - T_{cref}}{T_s}\right) = U_{BCref}$ $U_{CA} = U_{Cg} - U_{Ag} = V_{dc}\left(\frac{T_{cref} - T_e}{T_s}\right) = U_{CAref} - V_{dc}\left(\frac{T_{Aref} - T_e}{T_s}\right)$
i_A narrow, $i_A < 0$, $i_B > 0$, $i_C > 0$, $i_N < 0$	$U_{Ag} = V_{dc}\left(\frac{2T_e}{T_s}\right)$ $U_{Bg} = V_{dc}\left(\frac{T_{bref} - T_e}{T_s}\right)$ $U_{Cg} = V_{dc}\left(\frac{T_{cref} - T_e}{T_s}\right)$ $U_{Ng} = V_{dc}\left(\frac{T_{Nref} + T_e}{T_s}\right)$	$U_{AN} = U_{Ag} - U_{Ng} = V_{dc}\left(\frac{-T_{Nref} + T_e}{T_s}\right) = U_{ANref} - V_{dc}\left(\frac{T_{Aref} - T_e}{T_s}\right)$ $U_{BN} = U_{Bg} - U_{Ng} = V_{dc}\left(\frac{T_{bref} - T_{Nref} - 2T_e}{T_s}\right) = U_{BNref} - V_{dc}\left(\frac{2T_e}{T_s}\right)$ $U_{CN} = U_{Cg} - U_{Ng} = V_{dc}\left(\frac{T_{cref} - T_{Nref} - 2T_e}{T_s}\right) = U_{CNref} - V_{dc}\left(\frac{2T_e}{T_s}\right)$ $U_{AB} = U_{Ag} - U_{Bg} = V_{dc}\left(\frac{-T_{bref} + 3T_e}{T_s}\right) = U_{ABref} - V_{dc}\left(\frac{T_{Aref} - 3T_e}{T_s}\right)$ $U_{BC} = U_{Bg} - U_{Cg} = V_{dc}\left(\frac{T_{bref} - T_{cref}}{T_s}\right) = U_{BCref}$ $U_{CA} = U_{Cg} - U_{Ag} = V_{dc}\left(\frac{T_{cref} - 3T_e}{T_s}\right) = U_{CAref} + V_{dc}\left(\frac{T_{Aref} - 3T_e}{T_s}\right)$

By considering Table 16 the compensating times can be calculated as shown in Figure 5-15:

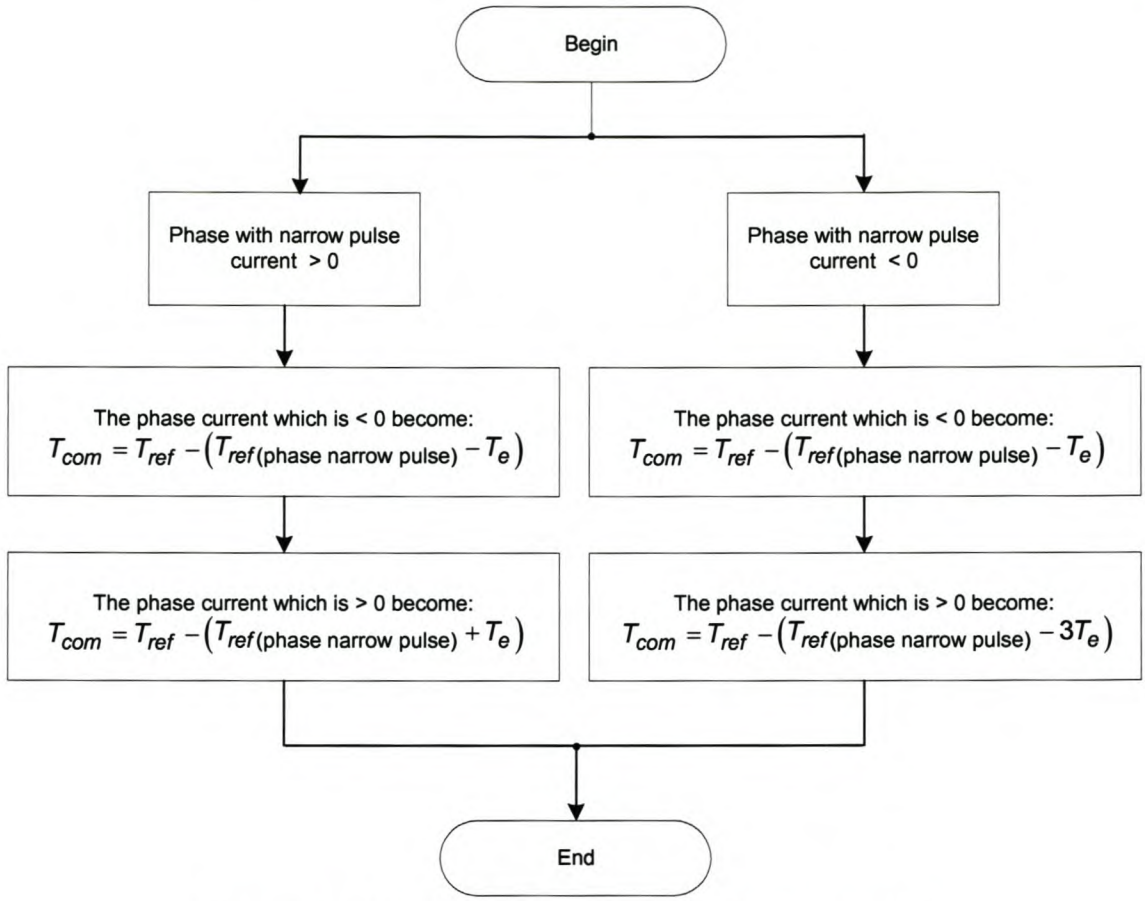


Figure 5-15 Calculation of compensating times for mode 2

5.3.4 Dead-time compensation during a current direction change

To explain the effect during a current direction change, consider Figure 5-16. When the current direction is bigger than 0, and in mode 1, the compensated reference duty cycle can be determined as:

$$T_{com} = T_{ref} + T_e \tag{5-14}$$

but when the current direction changes, the compensating current must be:

$$T_{com} = T_{ref} - T_e \tag{5-15}$$

in order to realise the correct reference voltage vector.

However, when the actual current is used in the dead-time compensation technique, the compensating technique will work incorrectly. The reason for this can best be explained by considering the following. When the actual current is larger than 0, and the reference current value changes direction, the dead-time compensating technique will prevent the actual current from changing direction. The actual current direction will only change when the newly applied T_{com} satisfies the following inequality:

$$T_{com(new)} < T_{com} - 2T_e \tag{5-16}$$

Alternatively, when the actual current is changing direction from a negative to positive value, it will only change its direction when the following inequality is satisfied:

$$T_{com(new)} > T_{com} + 2T_e \tag{5-17}$$

This process is illustrated graphically in Figure 5-16 when the actual current direction is changing from positive to negative:

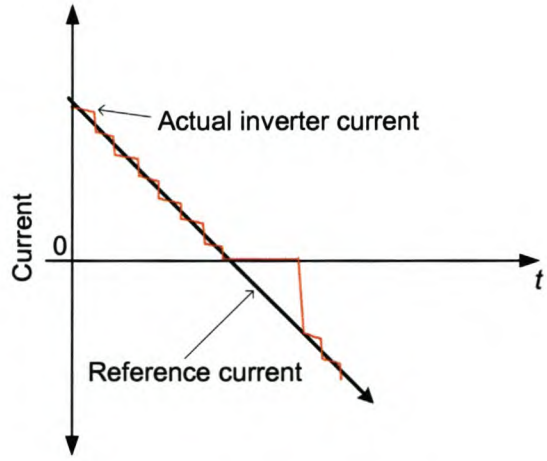


Figure 5-16 Illustrating the effect when reference current change direction

To overcome this effect during a current direction change, the reference currents must be used instead of the actual measured currents in order to achieve proper dead-time compensation.

5.3.5 Simulation results

The simulation results shown in Figure 5-17 use the prediction controller with time delay compensation implemented to investigate the effect that dead time has on the predictive current controller performance. Figure 5-17 shows the inverters' phase A (blue), phase B(green) and phase C (red) currents. The black traces are the sinusoidal reference current traces, as was used in Chapter 4, for the respective current components. Figure 5-17 (a) illustrates the effect that dead-time has on the performance of the predictive current controller when no dead-time compensation is implemented, Figure 5-17 (b) illustrates the performance of the predictive current controller when the actual current direction is used in the dead-time compensator, and in Figure 5-17 (c) the performance of the predictive current controller is illustrated when the reference current vector is used in the dead-time compensator. It can clearly be seen that the glitches in the waveforms are removed by using the reference current waveforms in the dead-time compensator.

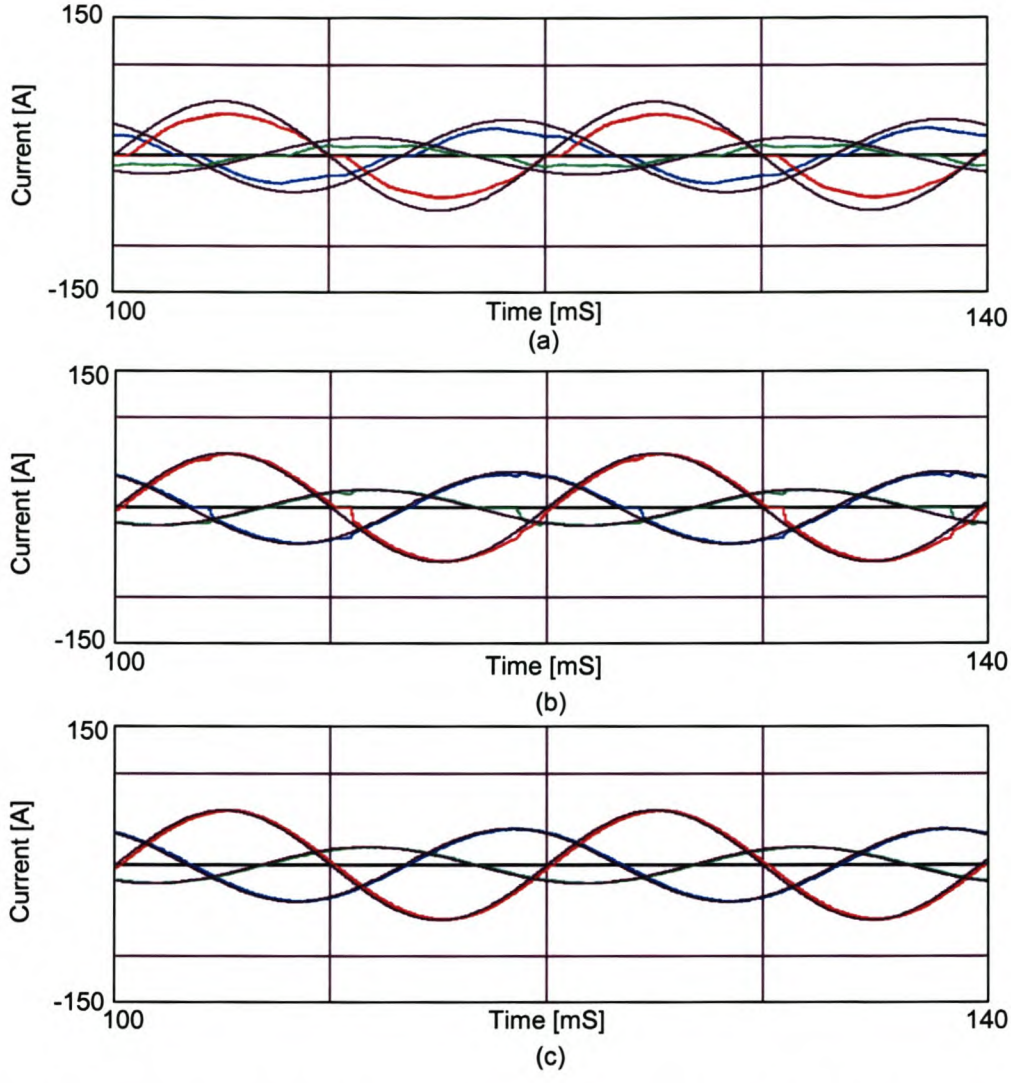


Figure 5-17 Predictive current controller with neutral conductor (a) no dead-time compensation (b) dead-time compensation using only the actual current directions (c) dead-time compensation using the reference current vector

5.4 Predictive current controller simulations using the proposed current controller algorithms

In Figure 5-18 (a), Figure 5-19 (a), Figure 5-20 (a) and Figure 5-21 (a) the reference current (black traces) and the actual currents (blue, red, green traces) are shown when the predictive current controller is implemented in a practical system with the proposed time delay and dead-time compensation algorithms implemented.

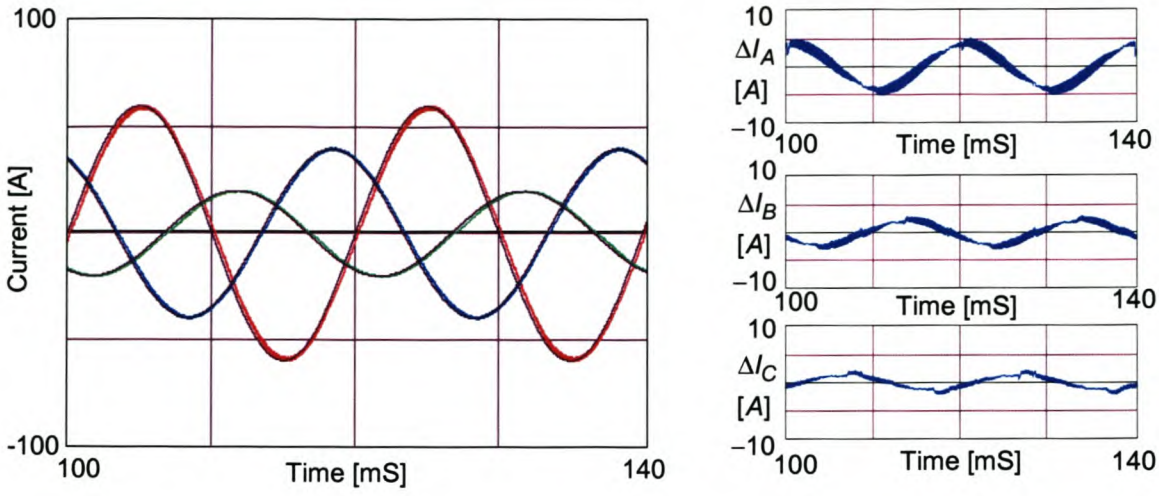


Figure 5-18 Predictive current controller without neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented.

Figure 5-18 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 2.9 A, 1.6 A and 1.1 A respectively.

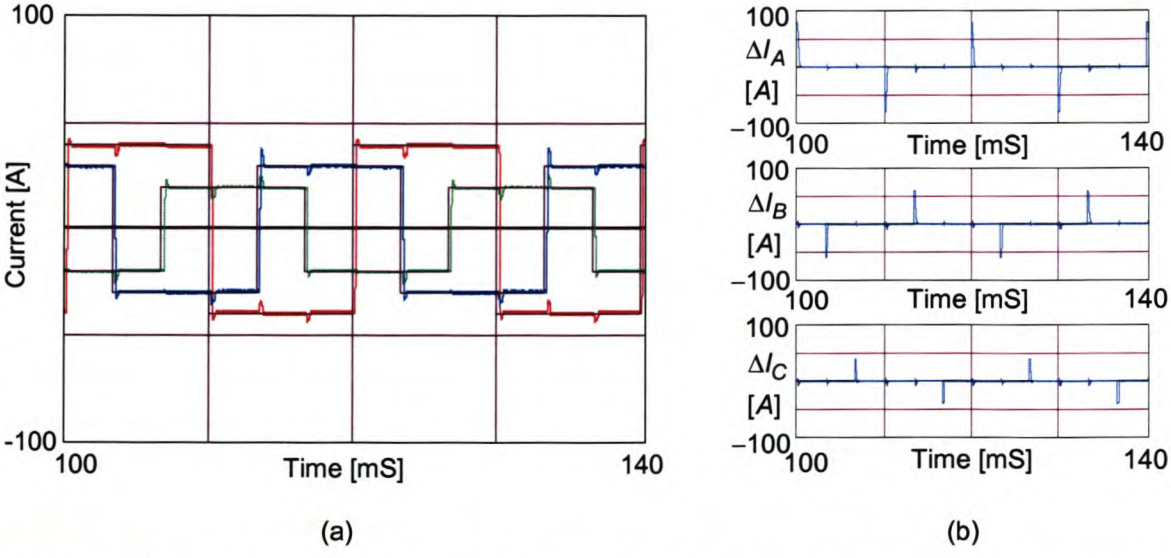


Figure 5-19 Predictive current controller without neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented.

Figure 5-19 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 11.1 A, 7.7 A and 4.8 A respectively.

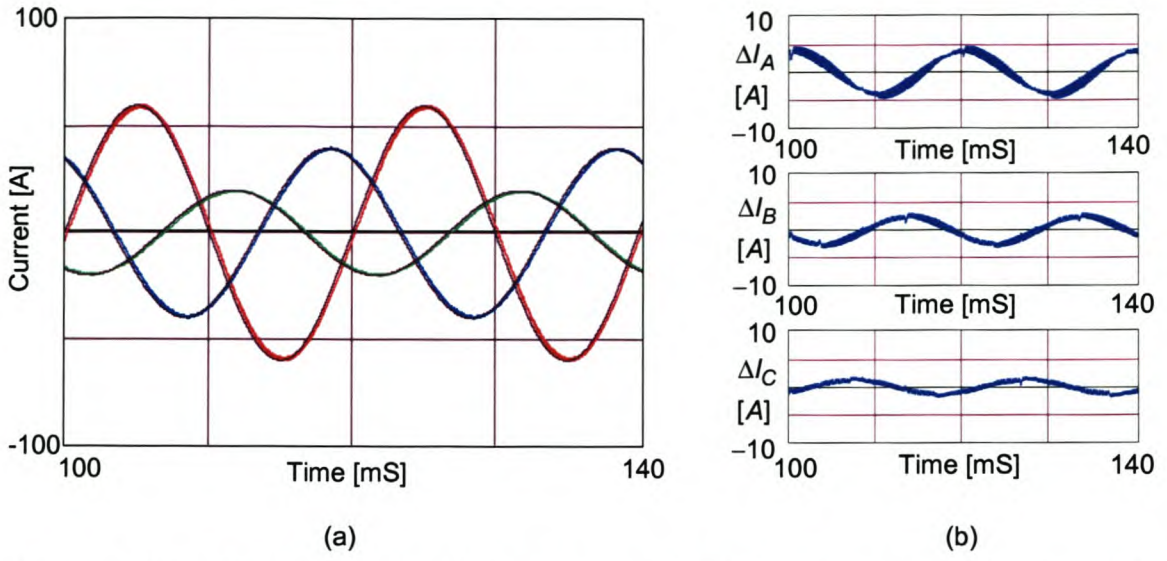


Figure 5-20 Predictive current controller with neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented.

Figure 5-20 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 2.8 A, 1.8 A and 1.0 A respectively.

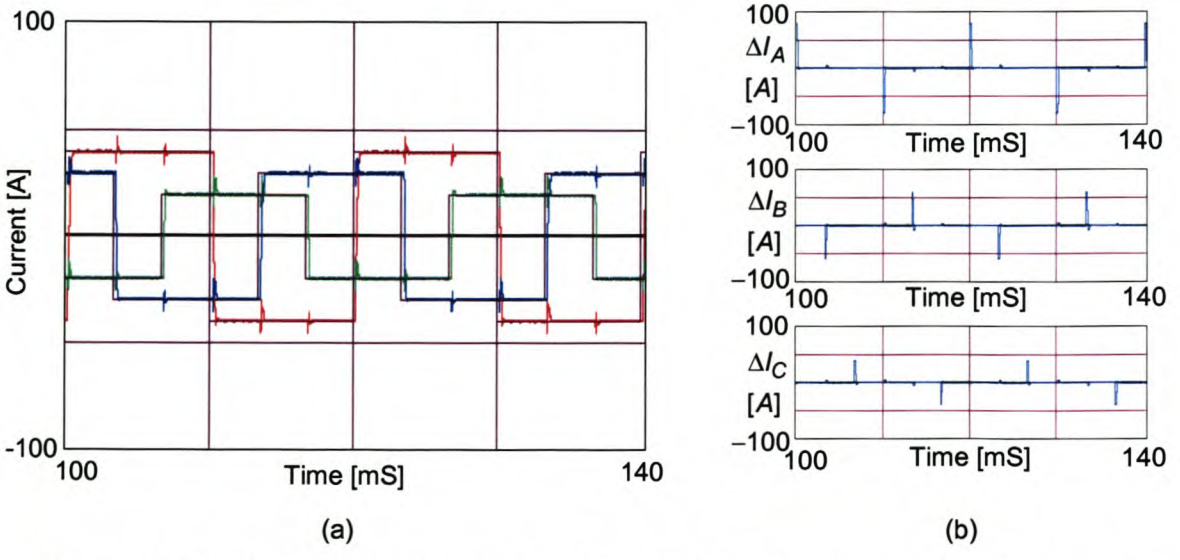


Figure 5-21 Predictive current controller with neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented.

Figure 5-21 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 10.5 A, 8.1 A and 5.6 A respectively.

From the above results can be seen that the predictive current controller work satisfactorily with the proposed compensating techniques implemented.

5.5 Sliding mode current controller simulations using the proposed current controller algorithms

This section will investigate the performance of the different types of sliding mode current controllers discussed in Chapter 4.

In Figure 5-22 (a), Figure 5-23 (a), Figure 5-24 (a) and Figure 5-25 (a) the reference current (black traces) and the actual currents (blue, red, green traces) are shown when the sliding mode current controller utilising the ideal saturating function as a reaching mode controller is implemented in a practical system with the proposed time delay and dead-time compensation algorithms implemented.

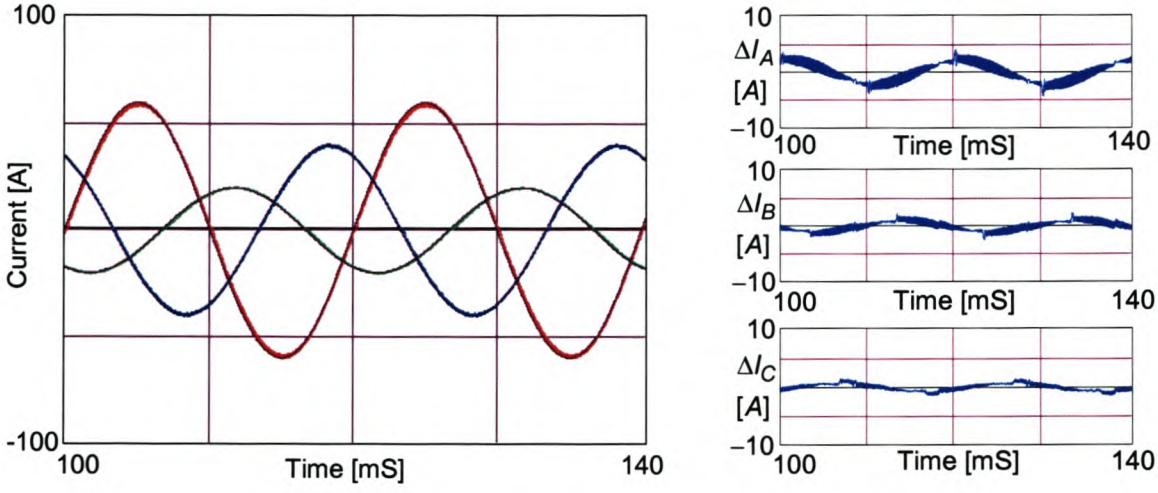


Figure 5-22 Ideal saturation controller without the neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented.

Figure 5-22 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 1.7 A, 0.8 A and 0.6 A respectively.

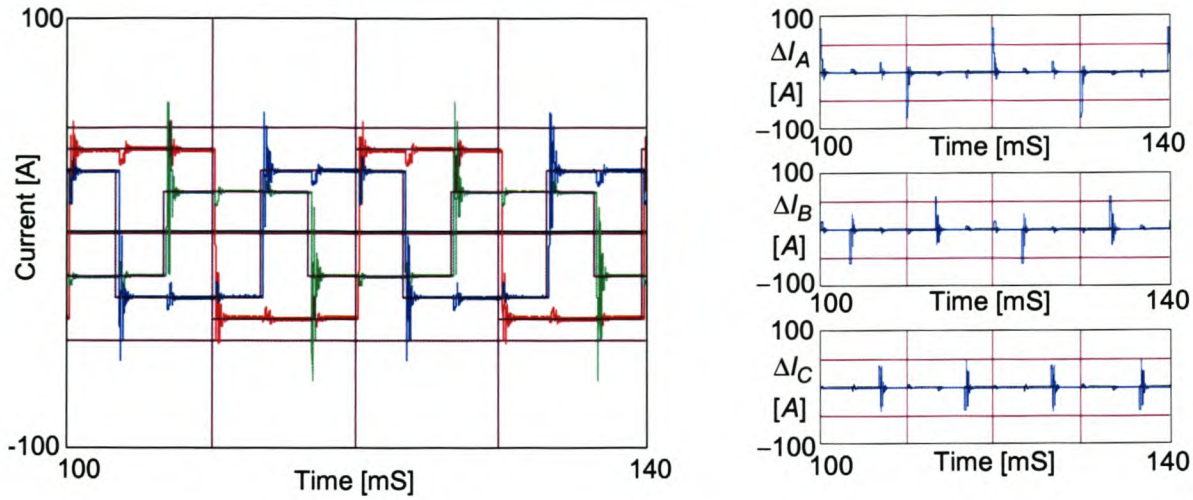


Figure 5-23 Ideal saturation controller without the neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented.

Figure 5-23 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 11.0 A, 7.9 A and 6.4 A respectively.

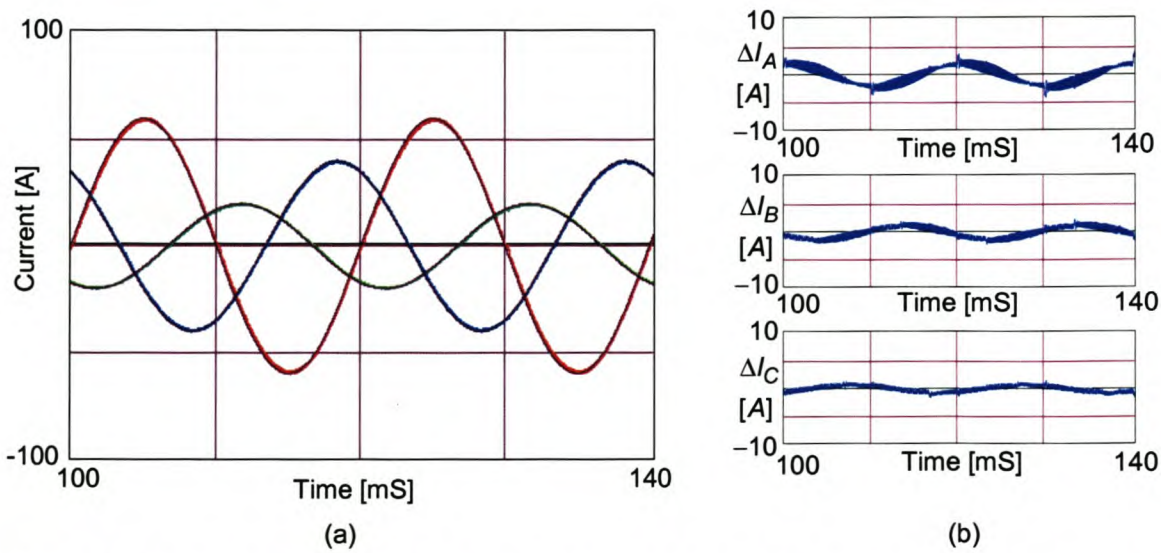


Figure 5-24 Ideal saturation controller with the neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented.

Figure 5-24 (b) show plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current error for phase A, phase B and phase C are 1.5 A, 0.9 A and 0.5 A respectively.

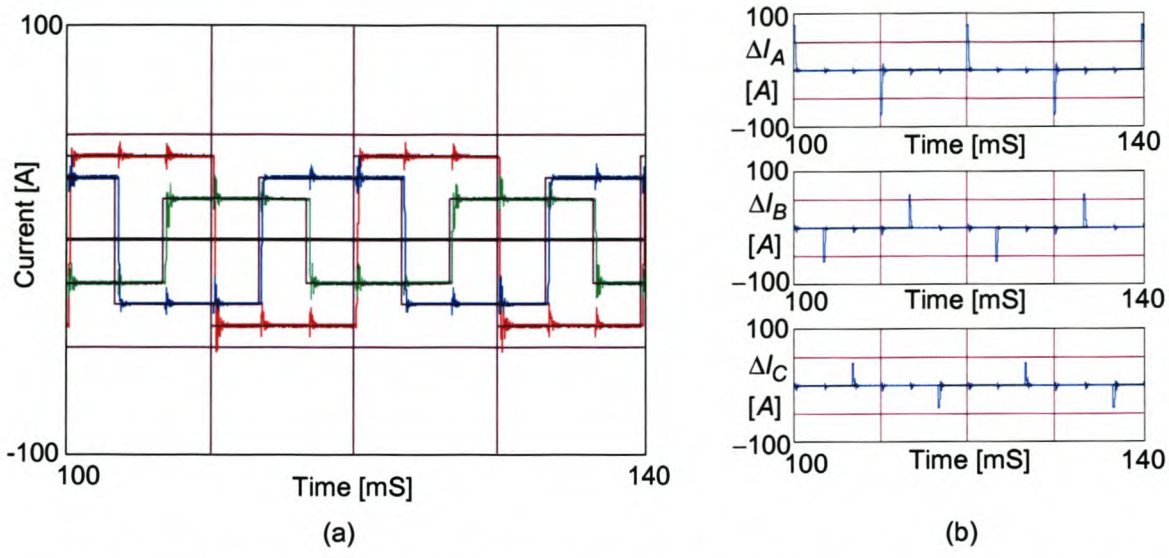


Figure 5-25 Ideal saturation controller with the neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented.

Figure 5-25 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 10.4 A, 8.2 A and 5.7 A respectively.

By considering the simulation results for the ideal saturating current controller, it can be seen that there is a large overshoot, when a sudden step change is applied to the reference current signal if the neutral inductor is not connected, and the overshoot is dampened when the neutral inductor is connected. This current control technique is suitable for high- and low-frequency reference current tracking when the neutral current is connected. However, care must be taken when using this type of current controller without the neutral inductor connected, because of the possible high overshoot when there is a sudden step in the reference currents.

In Figure 5-26 (a), Figure 5-27 (a), Figure 5-28 (a) and Figure 5-29 (a) the reference current (black traces) and the actual currents (blue, red, green traces) are shown when the sliding mode current controller utilising the constant rate controller as a reaching mode controller is implemented in a practical system with the proposed time delay and dead-time compensation algorithms implemented.

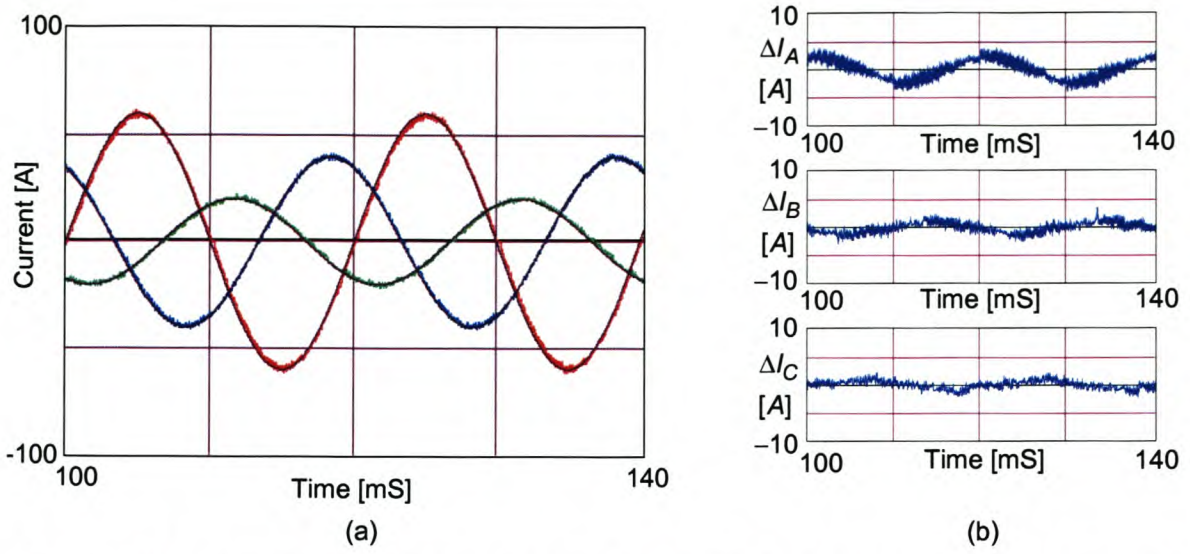


Figure 5-26 Constant rate controller without the neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented.

Figure 5-26 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 1.6 A, 0.8 A and 0.7 A respectively.

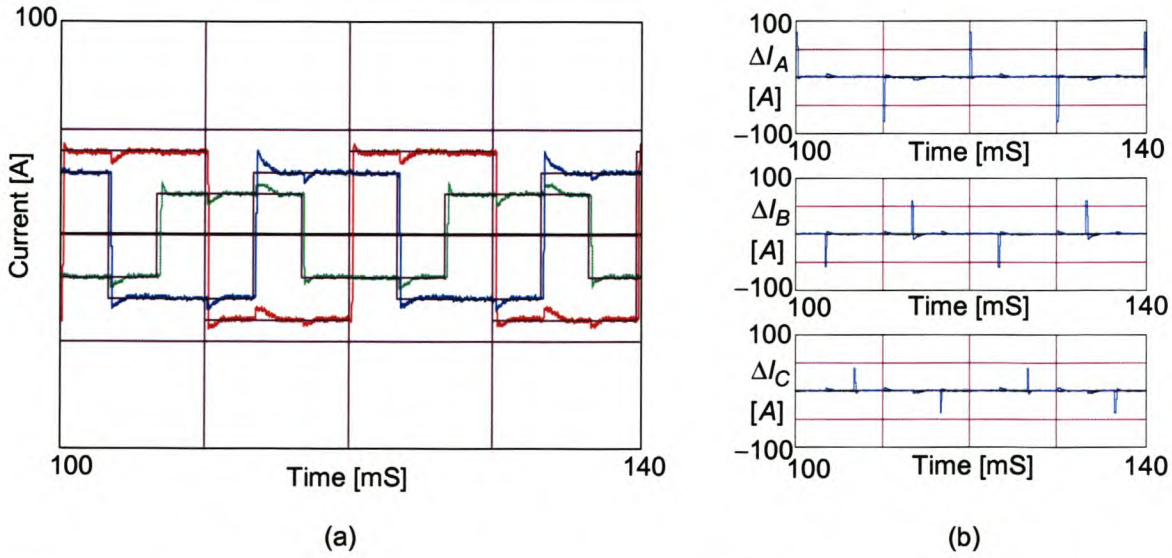


Figure 5-27 Constant rate controller without the neutral inductor connected, using square references, with time delay and dead-time compensation implemented.

Figure 5-27 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 9.8 A, 7.8 A and 5.6 A respectively.

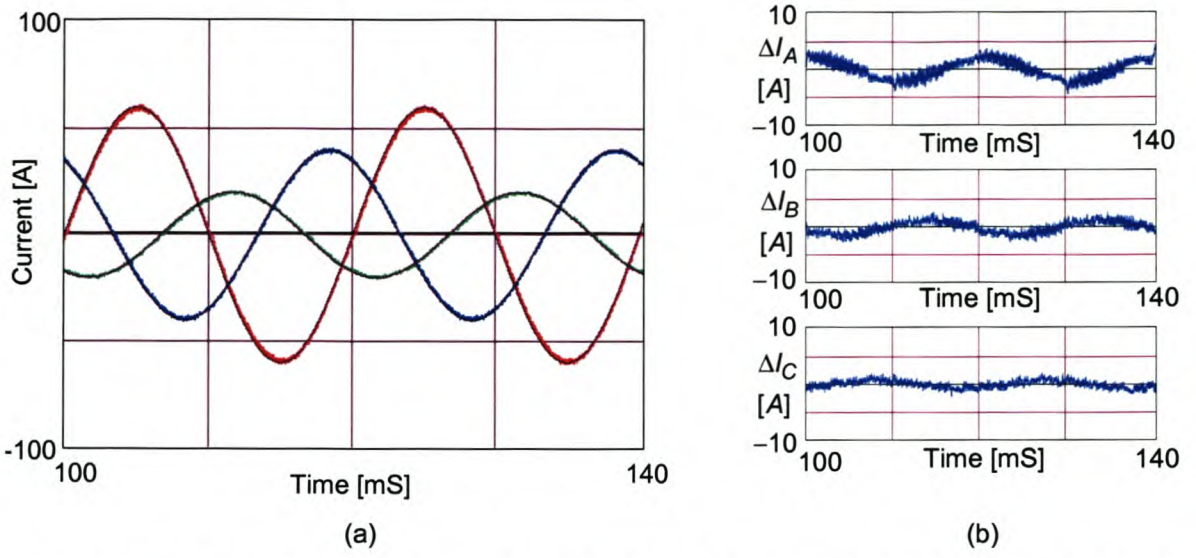


Figure 5-28 Constant rate controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented.

Figure 5-28 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 1.6 A, 1.0 A and 0.8 A respectively.

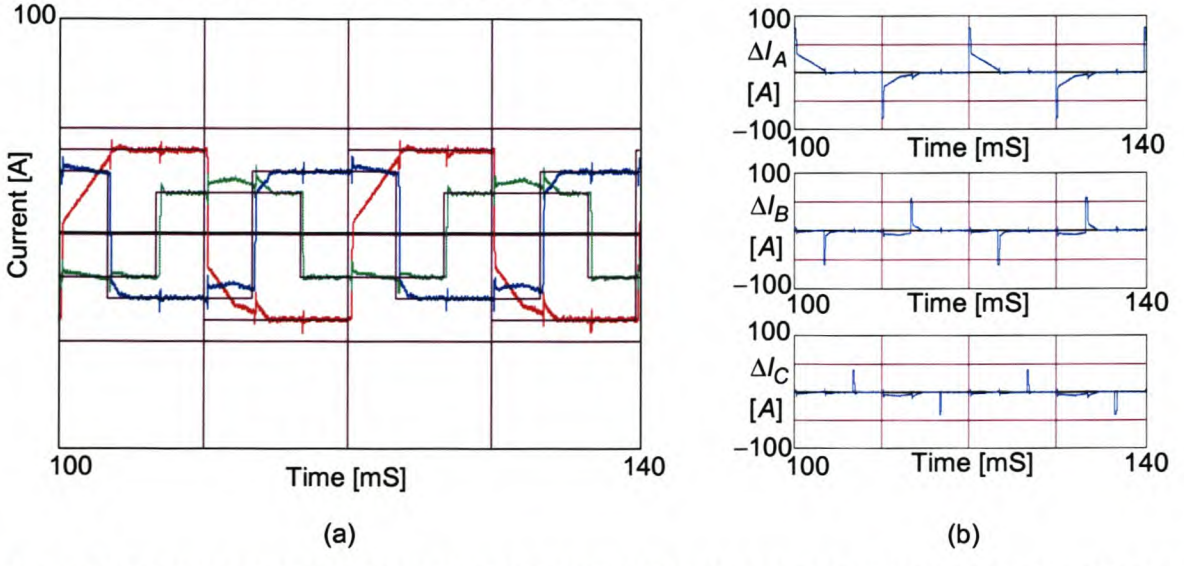


Figure 5-29 Constant rate controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented.

Figure 5-29 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 15.0 A, 8.9 A and 5.7 A respectively.

As can be seen in Figure 5-26 and Figure 5-28, the constant rate controller tracks low-frequency components very well. In Figure 5-27 can be seen that the constant rate controller tracks the high frequency reference signals satisfactorily when the neutral inductor is not connected. The constant rate controller is, however, not suitable for reference current tracking of high frequency components when the neutral inductor is connected, since it needs a higher gain when high-frequency components are tracked. This is illustrated in Figure 5-29. The gains in the constant rate current controller can be increased, but

this in turn has a detrimental effect on the low-frequency tracking ability due to the large overshoots that will arise.

In Figure 5-30 (a), Figure 5-31 (a), Figure 5-32 (a) and Figure 5-33 (a) the reference current (black traces) and the actual currents (blue, red, green traces) are shown when the sliding mode current controller utilising the constant rate plus proportional controller as a reaching mode controller is implemented in a practical system with the proposed time delay and dead-time compensation algorithms implemented.

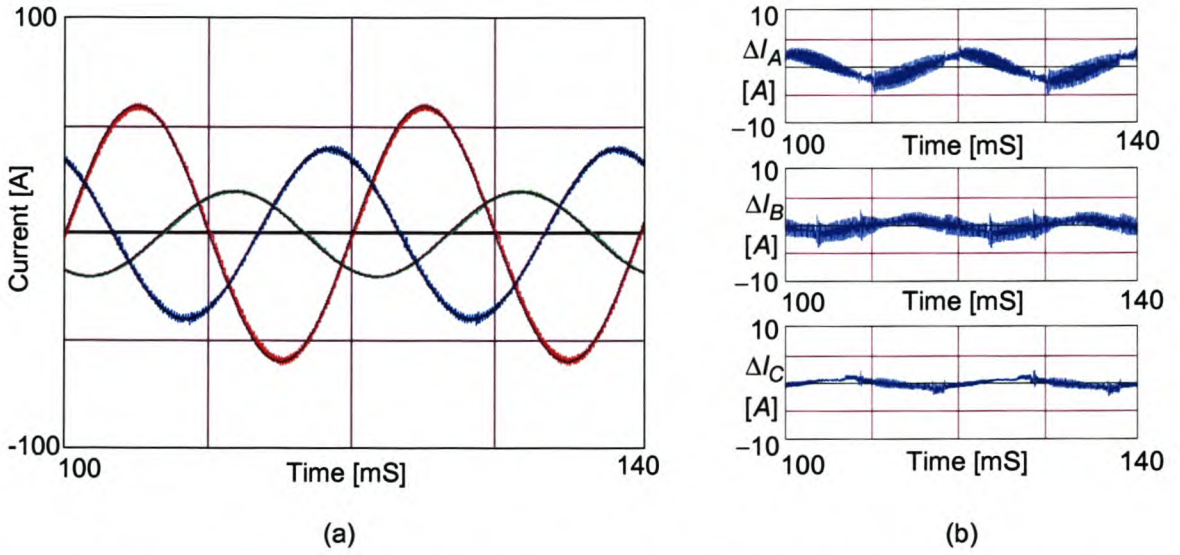


Figure 5-30 Constant rate plus proportional controller without the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented.

Figure 5-30 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 1.7 A, 1.1 A and 0.7 A respectively.

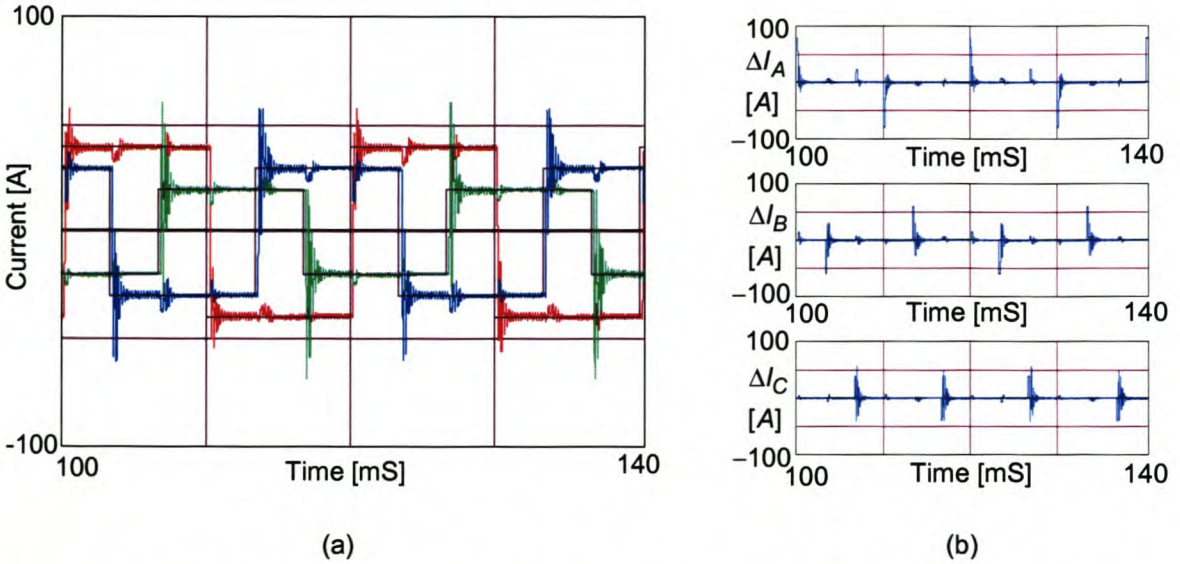


Figure 5-31 Constant rate plus proportional controller without the neutral inductor connected, using square references, with time delay and dead-time compensation implemented.

Figure 5-31 (b) show plots of the current errors between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 11.3 A, 8.5 A and 7.5 A respectively.

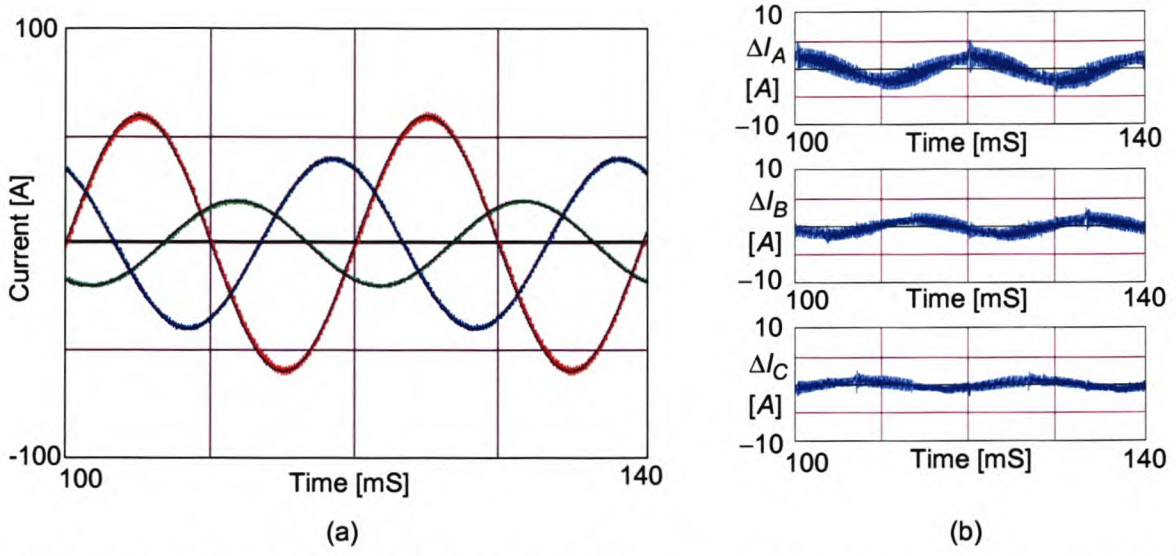


Figure 5-32 Constant rate plus proportional controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented.

Figure 5-32 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 1.6 A, 1.2 A and 0.6 A respectively.

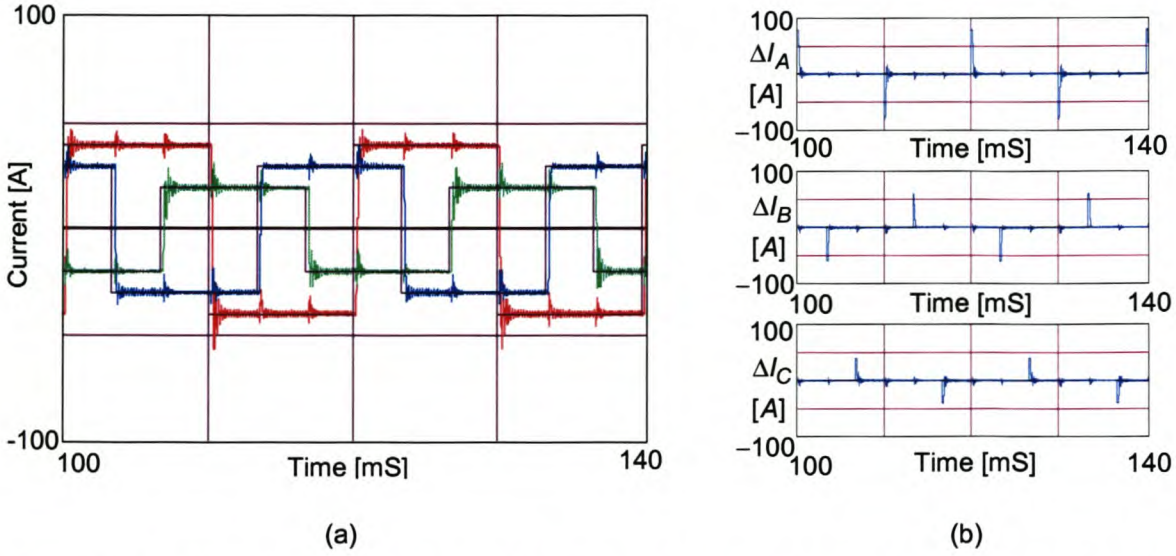


Figure 5-33 Constant rate plus proportional controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented.

Figure 5-33 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 11.3 A, 7.7 A and 5.5 A respectively.

The constant rate plus proportional current controller offers a solution to the shortcomings of the constant rate controller since it offers a low constant gain for the proper tracking of the low-frequency reference current components, and a high proportional gain for the proper tracking of the high-frequency reference current components. This technique is well suited for controllers with the neutral inductor connected, but its performance is lacking due to the large overshoot when the neutral inductor is not connected.

5.6 Shunt active power filter simulations utilising the proposed controllers

This section will implement the discussed current controllers in a shunt active power filter application. The simulation model that is used in the simulation is shown in Appendix C-2. The extended synchronous reference frame technique discussed in Chapter 3 will be used to generate the reference current signals.

5.6.1 Predictive current controller without the neutral inductor connected

Figure 5-34 (a) and Figure 5-34 (b) illustrate the phase A (blue trace), B (red trace), and C (green trace) load currents and the phase A (blue trace), B (red trace) and C (green trace) source currents after compensation respectively. The load currents produce a negative sequence unbalance of 50% and a zero sequence unbalance of 50%. After compensation the negative sequence unbalance is reduced to 3.7%, and the zero sequence unbalance is reduced to 3.1%. The phase A and B source currents have a TDD of 49.2% before compensation and after compensation the TDD for phase A is reduced to 10.1%, phase B to 11.0% and phase C to 1.4%.

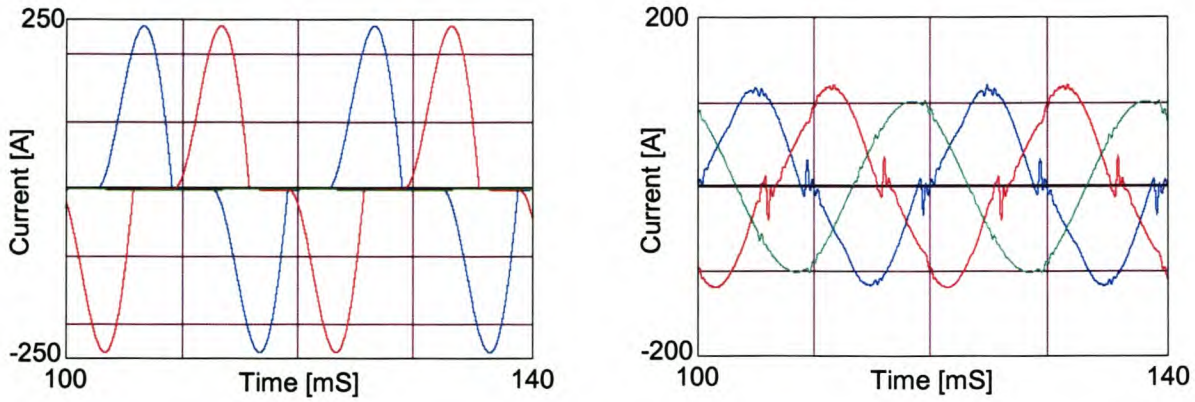


Figure 5-34 Simulation results showing (a) load current, and (b) compensated source currents

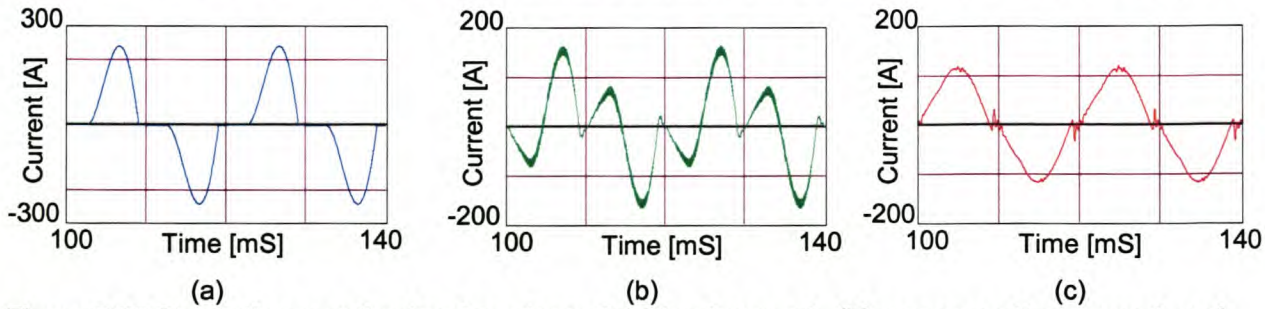


Figure 5-35 Simulation results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

Figure 5-35 (a) shows the load current, and Figure 5-35 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 5-35 (c).

Figure 5-36 (a) shows the uncompensated neutral current, and Figure 5-36 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 5-36 (c).

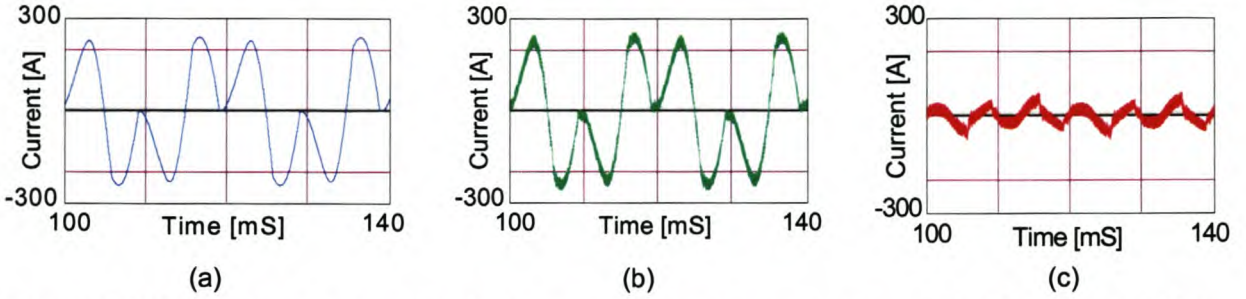


Figure 5-36 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 5-37 (a) and Figure 5-37 (b) show the phase A source current and the Phase A supply voltage before and after compensation respectively. From this it can be seen that reactive power compensation is achieved.

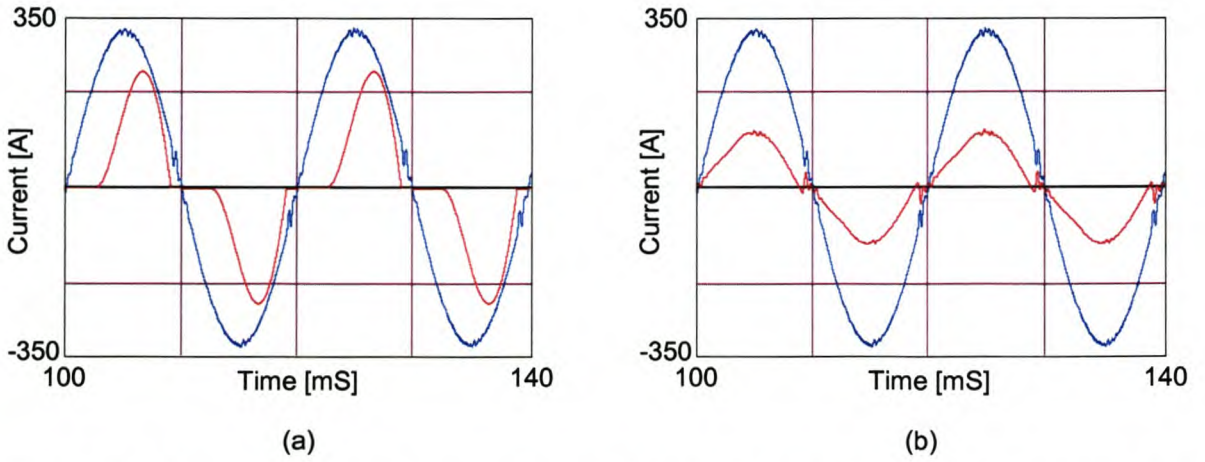


Figure 5-37 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace)

From the above simulation results can be seen that the shunt active power filter utilising the predictive current controller with time delay and dead-time compensation work satisfactorily.

5.6.2 Predictive current controller with the neutral inductor connected

Figure 5-38 (a) and Figure 5-38 (b) illustrate the phase A (blue trace), B (red trace), and C (green trace) load currents and the phase A (blue trace), B (red trace) and C (green trace) source currents after compensation respectively. The load currents produce a negative sequence unbalance of 50% and a zero sequence unbalance of 50%. After compensation the negative sequence unbalance is reduced to 3.3%, and the zero sequence unbalance is reduced to 3.6%. The phase A and B source currents have a TDD of 49.2% before compensation and after compensation the TDD for phase A is reduced to 10.9%, phase B to 11.1% and phase C to 1.2%.

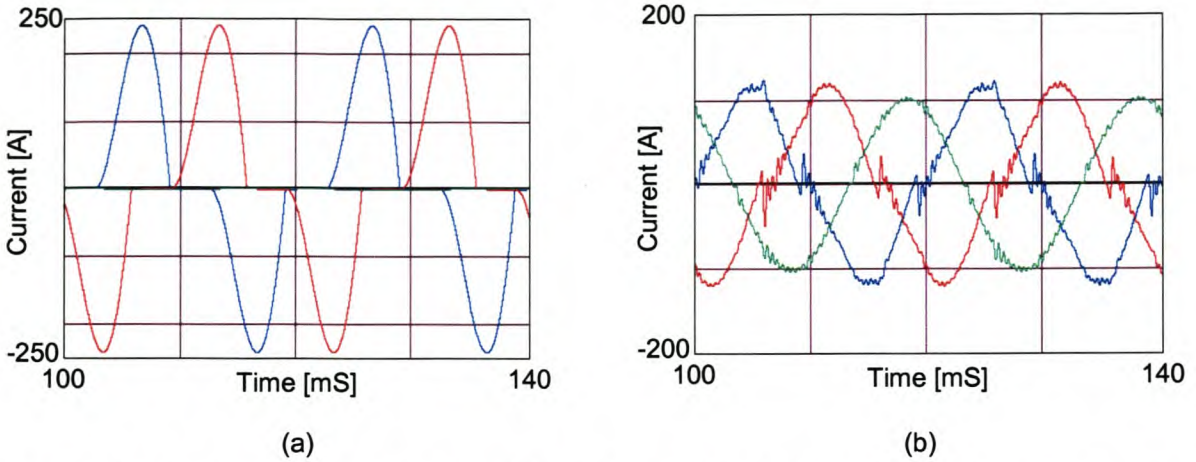


Figure 5-38 Simulation results showing (a) load current, and (b) compensated source currents

Figure 5-39 (a) shows the load current, and Figure 5-39 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 5-39 (c).

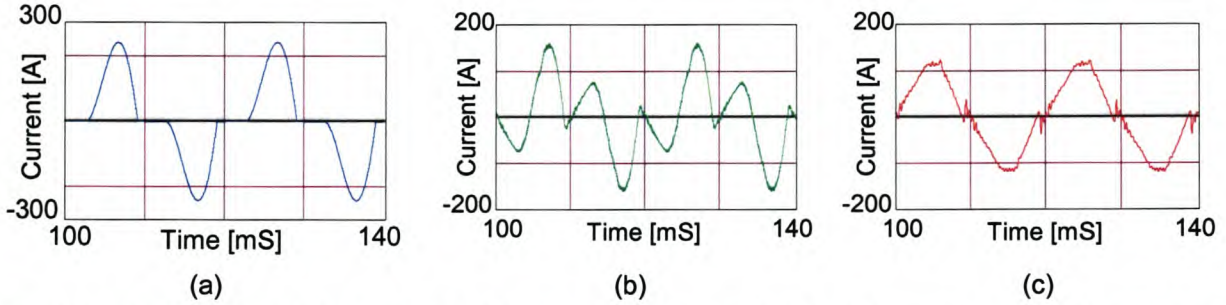


Figure 5-39 Simulation results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

Figure 5-40 (a) shows the uncompensated neutral current, and Figure 5-40 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 5-40 (c).

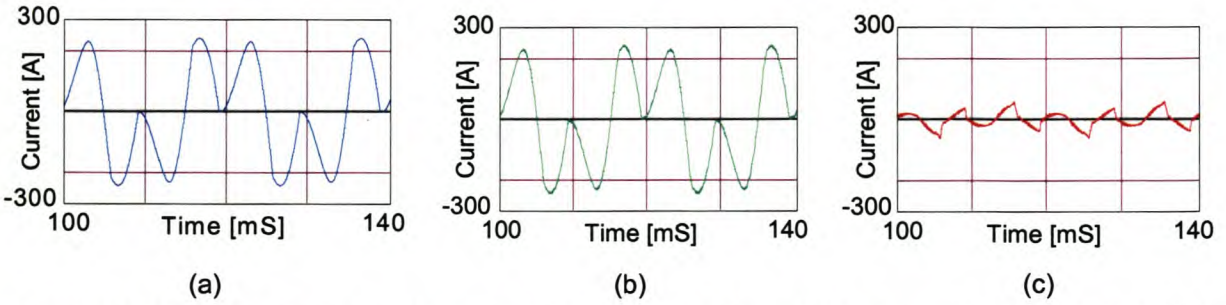


Figure 5-40 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 5-41 (a) and Figure 5-41 (b) shows the phase A source current and the phase A supply voltage before and after compensation respectively. From this it can be seen that reactive power compensation is achieved.

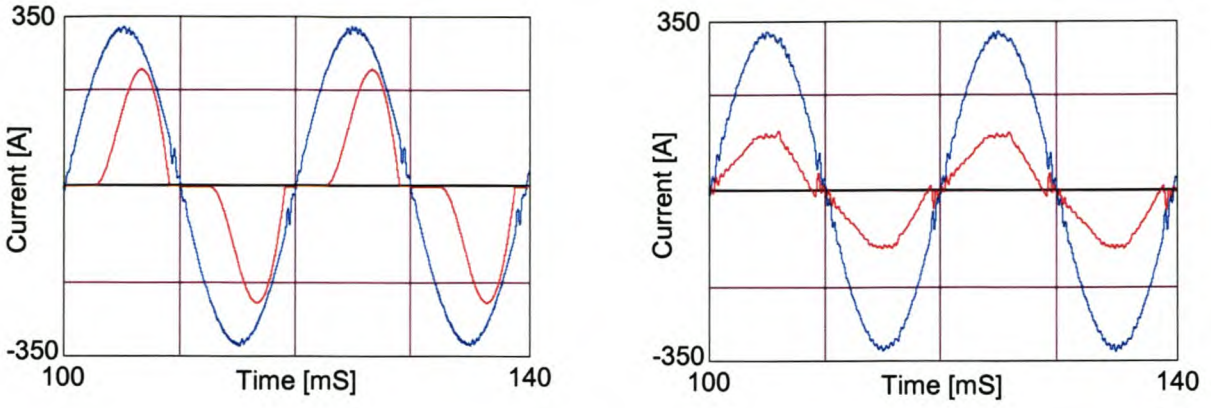


Figure 5-41 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace)

From the above simulation results can be seen that the shunt active power filter utilising the predictive current controller with time delay and dead-time compensation work satisfactorily.

5.6.3 Ideal saturating current controller without the neutral inductor connected

Figure 5-42 (a) and Figure 5-42 (b) illustrate the phase A (blue trace), B (red trace), and C (green trace) load currents and the phase A (blue trace), B (red trace), and C (green trace) source currents after compensation respectively. The load currents produce a negative sequence unbalance of 50% and a zero sequence unbalance of 50%. After compensation the negative sequence unbalance is reduced to 2.1%, and the zero sequence unbalance is reduced to 1.7%. The phase A and B source currents have a TDD of 49.2% before compensation and after compensation the TDD for phase A is reduced to 5.6%, phase B to 6.7% and phase C to 1.7%.

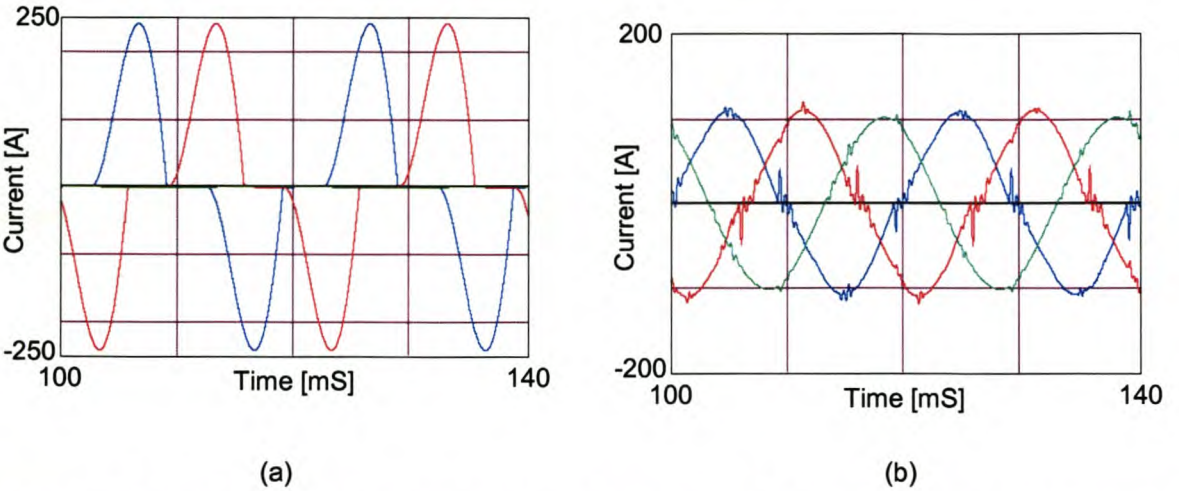


Figure 5-42 Simulation results showing (a) load current, and (b) compensated source currents

Figure 5-43 (a) shows the load current, and Figure 5-43 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 5-43 (c).

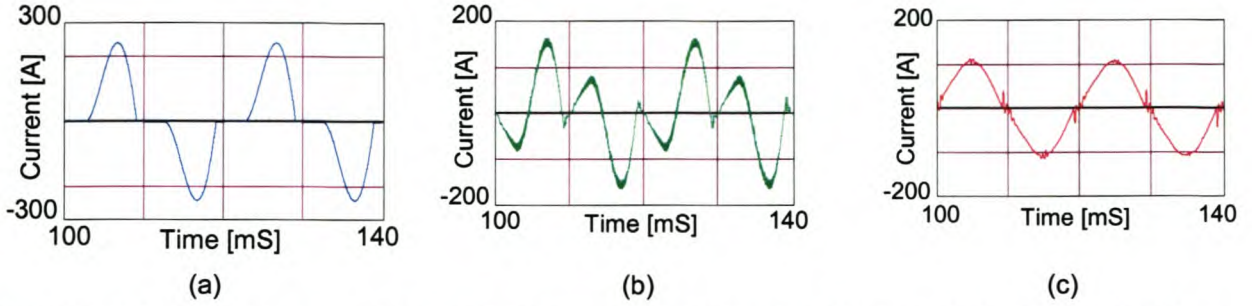


Figure 5-43 Simulation results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

Figure 5-44 (a) shows the uncompensated neutral current, and Figure 5-44 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 5-44 (c).

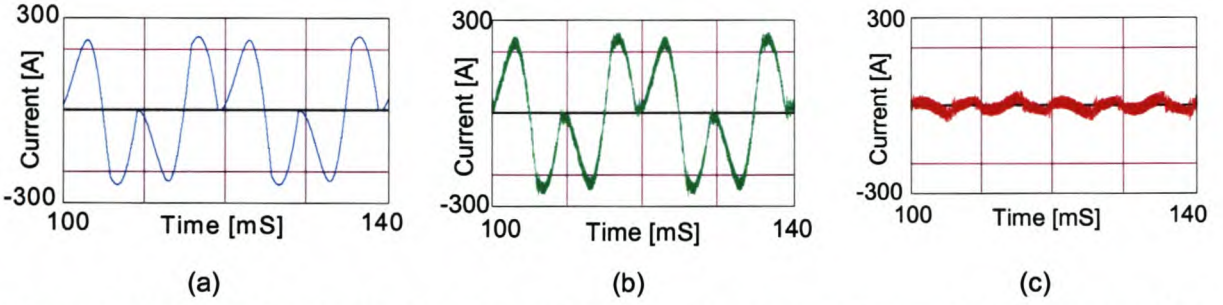


Figure 5-44 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 5-45 (a) and Figure 5-45 (b) shows the phase A source current and the phase A supply voltage before and after compensation respectively. From this it can be seen that reactive power compensation is achieved.

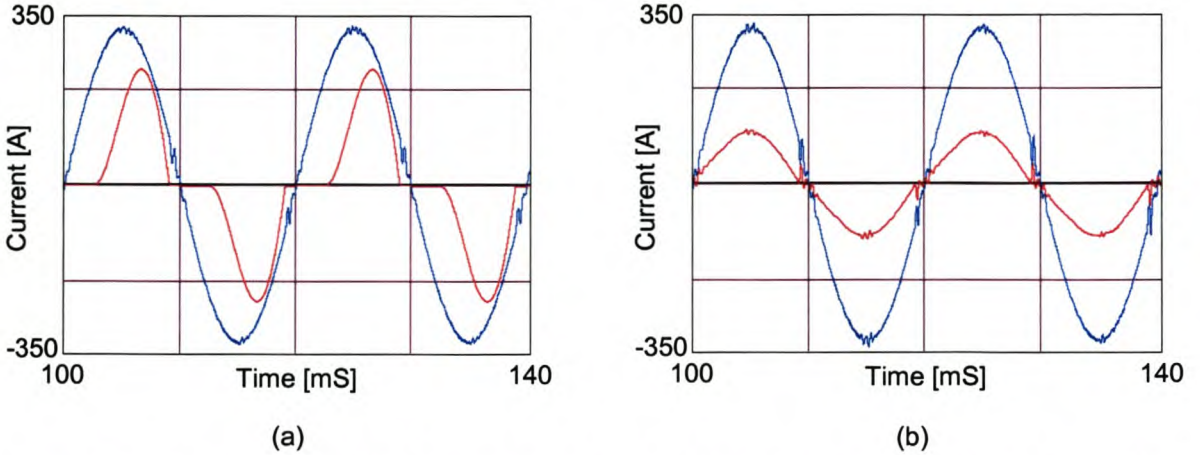


Figure 5-45 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace)

From the above simulation results can be seen that the shunt active power filter utilising the ideal saturating sliding mode current controller with time delay and dead-time compensation work satisfactorily.

5.6.4 Ideal saturating current controller with the neutral inductor connected

Figure 5-46 (a) and Figure 5-46 (b) illustrate the phase A (blue trace), B (red trace), and C (green trace) load currents and the phase A (blue trace), B (red trace) and C (green trace) source currents after compensation respectively. The load currents produce a negative sequence unbalance of 50% and a zero sequence unbalance of 50%. After compensation the negative sequence unbalance is reduced to 1.5%, and the zero sequence unbalance is reduced to 2.2%. The phase A and B source currents have a TDD of 49.2% before compensation and after compensation the TDD for phase A is reduced to 6.7%, phase B to 6.4% and phase C to 1.6%.

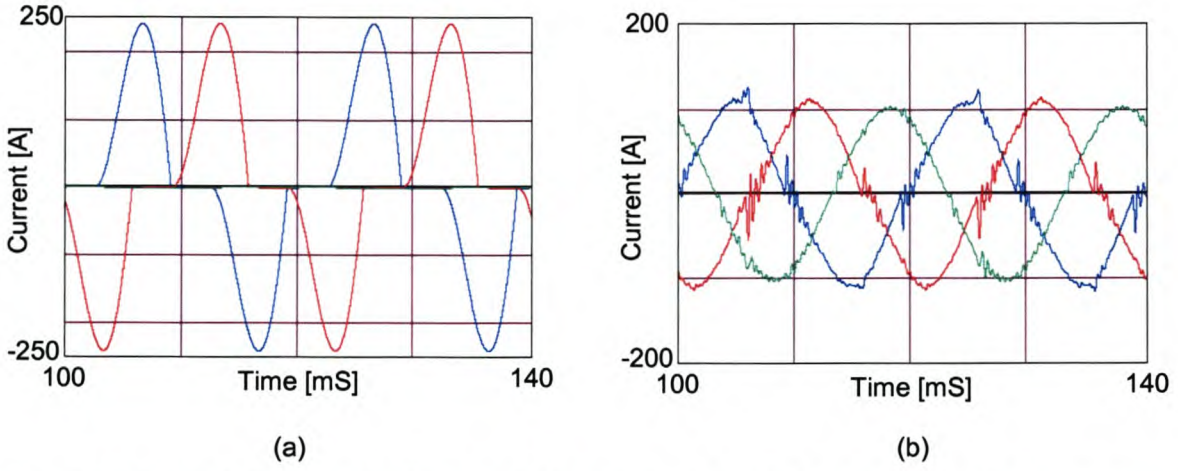


Figure 5-46 Simulation results showing (a) load current, and (b) compensated source currents

Figure 5-47 (a) shows the load current, and Figure 5-47 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 5-47 (c).

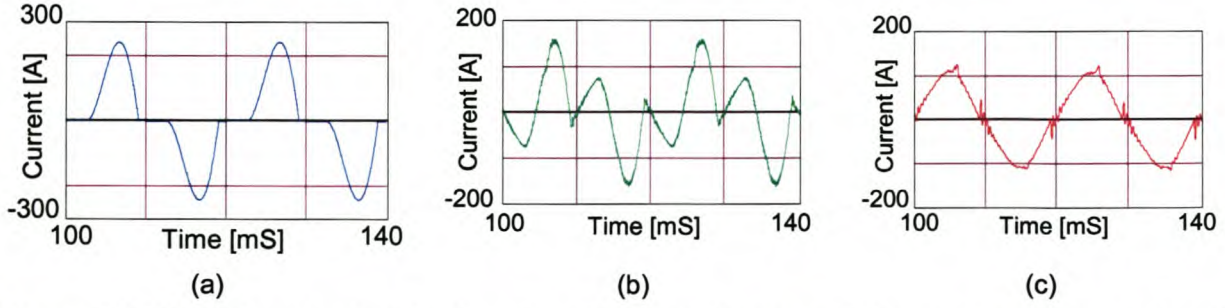


Figure 5-47 Simulation results showing phase A (a) Load current, (b) compensating current, and (c) compensated source current

Figure 5-48 (a) shows the uncompensated neutral current, and Figure 5-48 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 5-48 (c).

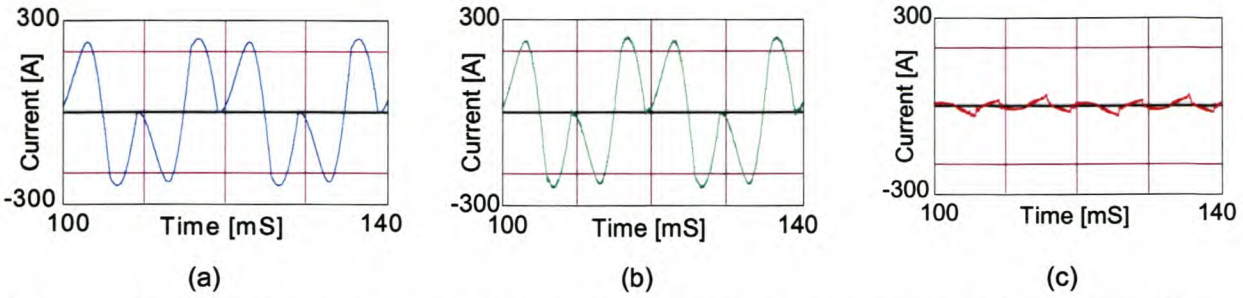


Figure 5-48 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 5-49 (a) and Figure 5-49 (b) shows the phase A source current and the phase A supply voltage before and after compensation respectively. From this it can be seen that reactive power compensation is achieved.

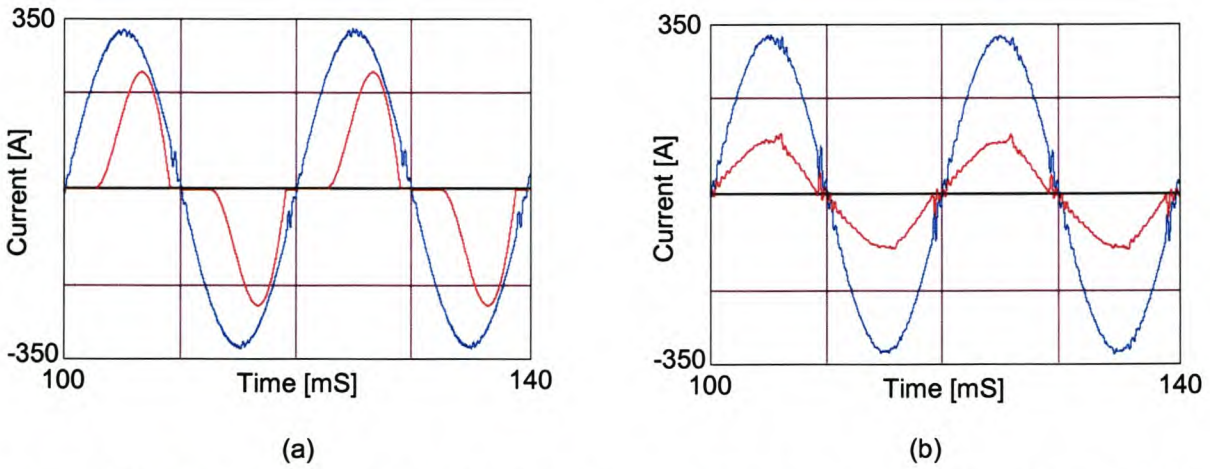


Figure 5-49 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace)

From the above simulation results can be seen that the shunt active power filter utilising the ideal saturating sliding mode current controller with time delay and dead-time compensation work satisfactorily.

5.6.5 Constant rate current controller without the neutral inductor connected

Figure 5-50 (a) and Figure 5-50 (b) illustrate the phase A (blue trace), B (red trace), and C (green trace) load currents and the phase A (blue trace), B (red trace), and C (green trace) source currents after compensation respectively. The load currents produce a negative sequence unbalance of 50% and a zero sequence unbalance of 50%. After compensation the negative sequence unbalance is reduced to 2.1%, and the zero sequence unbalance is reduced to 2.8%. The phase A and B source currents have a TDD of 49.2% before compensation and after compensation the TDD for phase A is reduced to 13.2%, phase B to 10.9% and phase C to 5.1%.

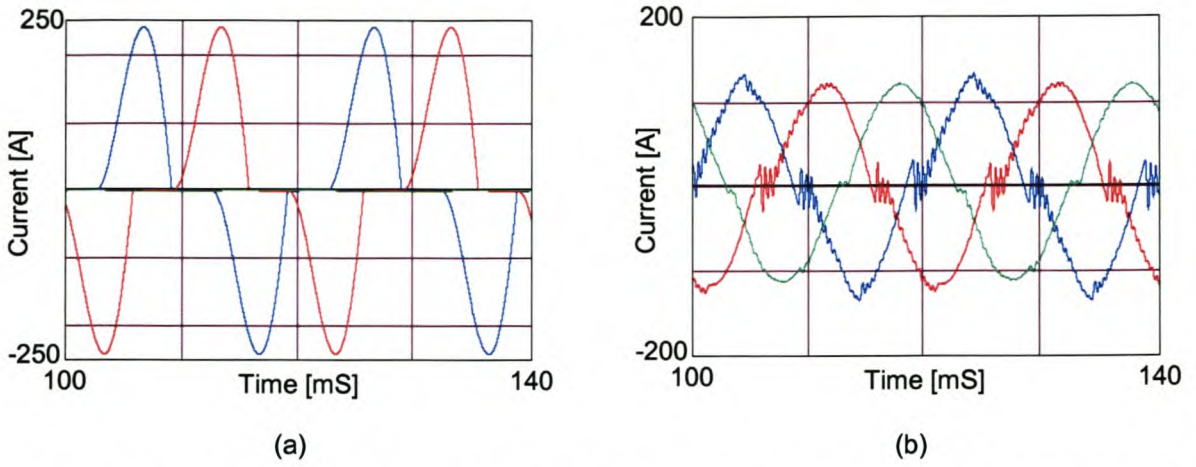


Figure 5-50 Simulation results showing (a) load current, and (b) compensated source currents

Figure 5-51 (a) shows the load current, and Figure 5-51 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 5-51 (c).

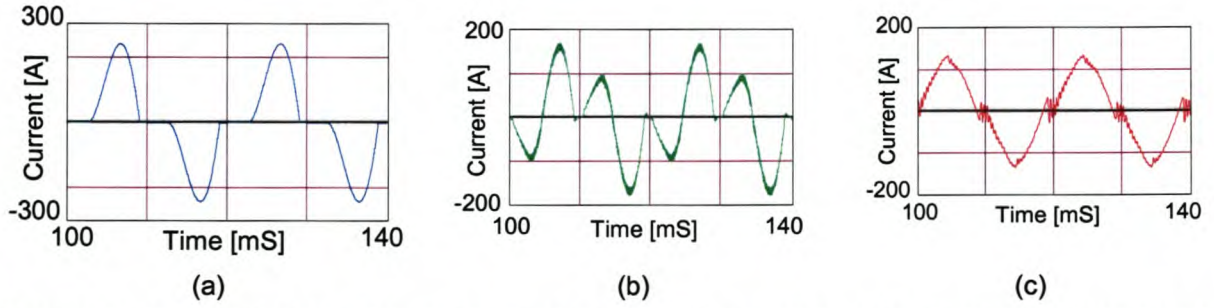


Figure 5-51 Simulation results showing phase A (a) Load current, (b) compensating current, and (c) compensated source current

Figure 5-52 (a) shows the uncompensated neutral current, and Figure 5-52 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 5-52 (c).

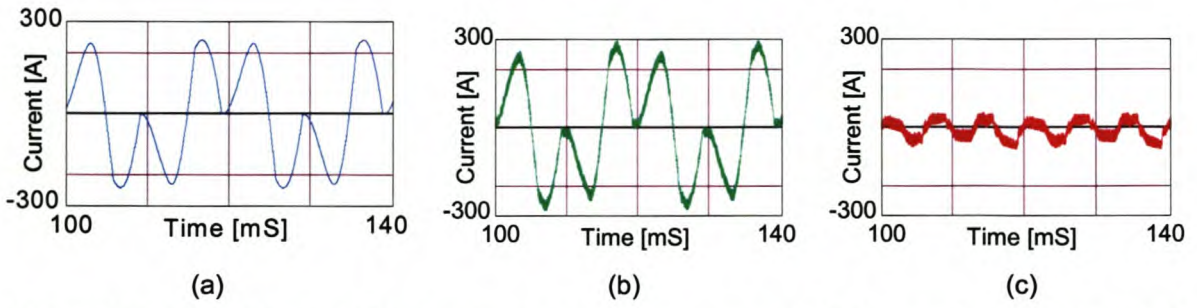


Figure 5-52 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 5-53 (a) and Figure 5-53 (b) shows the phase A source current and the phase A supply voltage before and after compensation respectively. From this it can be seen that reactive power compensation is achieved.

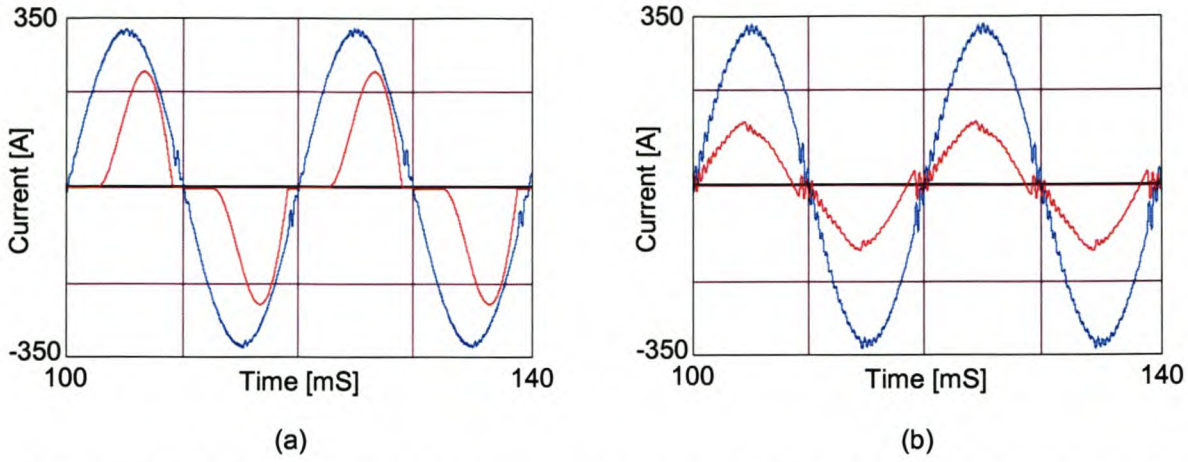


Figure 5-53 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace)

From the above simulation results can be seen that the shunt active power filter utilising the constant rate sliding mode current controller with time delay and dead-time compensation work satisfactorily.

5.6.6 Constant rate current controller with the neutral inductor connected

Figure 5-54 (a) and Figure 5-54 (b) illustrate the phase A (blue trace), B (red trace), and C (green trace) load currents and the phase A (blue trace), B (red trace), and C (green trace) source currents after compensation respectively. The load currents produce a negative sequence unbalance of 50% and a zero sequence unbalance of 50%. After compensation the negative sequence unbalance is reduced to 0.8%, and the zero sequence unbalance is reduced to 3.3%. The phase A and B source currents have a TDD of 49.2% before compensation and after compensation the TDD for phase A is reduced to 10.5%, phase B to 9.5% and phase C to 3.8%.

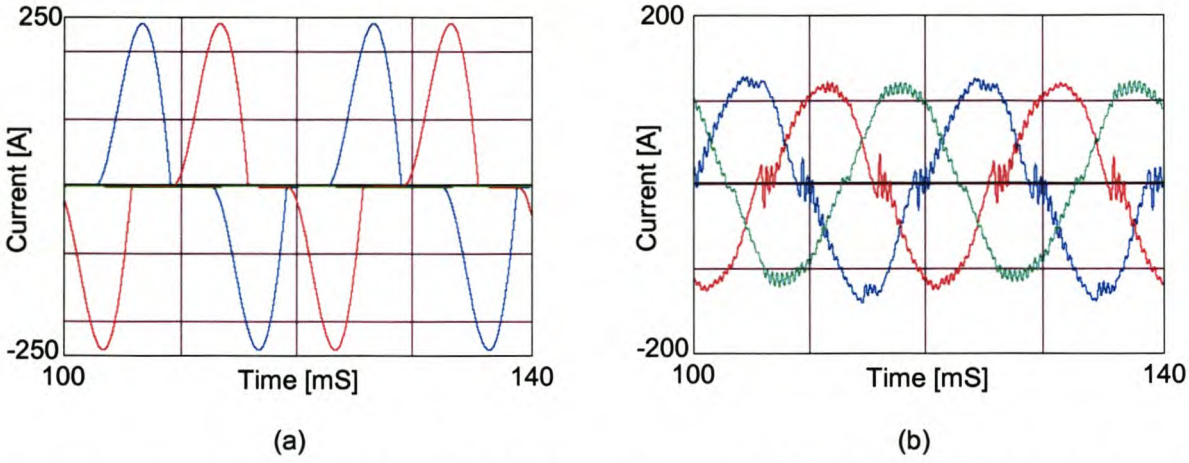


Figure 5-54 Simulation results showing (a) load current, and (b) compensated source currents

Figure 5-55 (a) shows the load current, and Figure 5-55 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 5-55 (c).

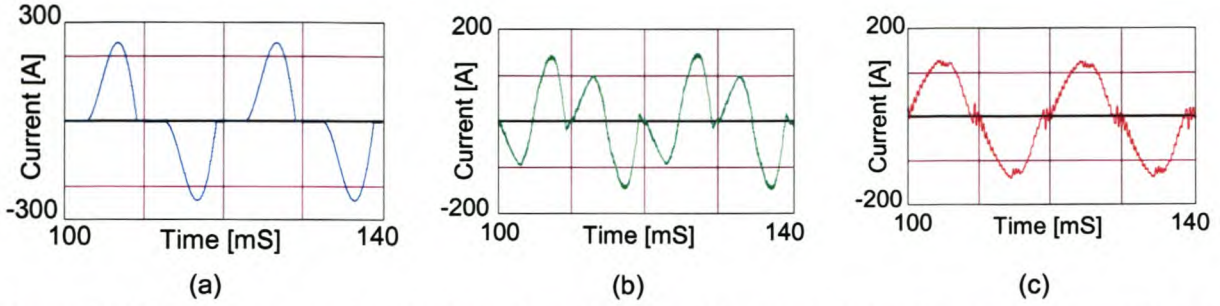


Figure 5-55 Simulation results showing phase A (a) Load current, (b) compensating current, and (c) compensated source current

Figure 5-56 (a) shows the uncompensated neutral current, and Figure 5-56 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 5-56(c).

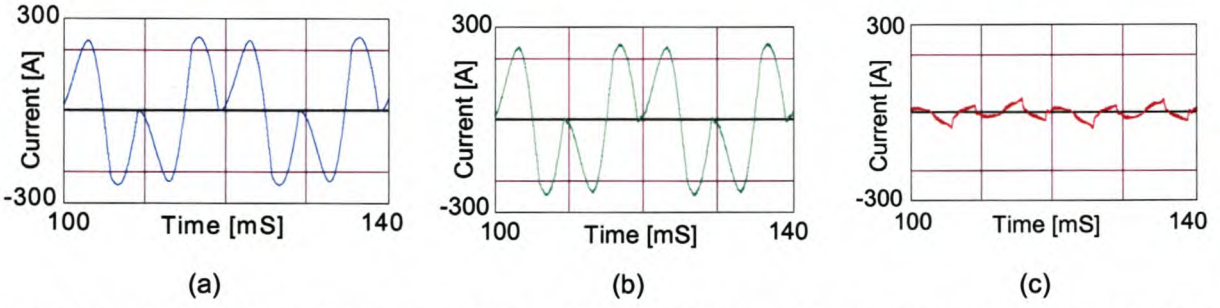


Figure 5-56 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 5-57 (a) and Figure 5-57 (b) shows the phase A source current and the phase A supply voltage before and after compensation respectively. From this it can be seen that reactive power compensation is achieved.

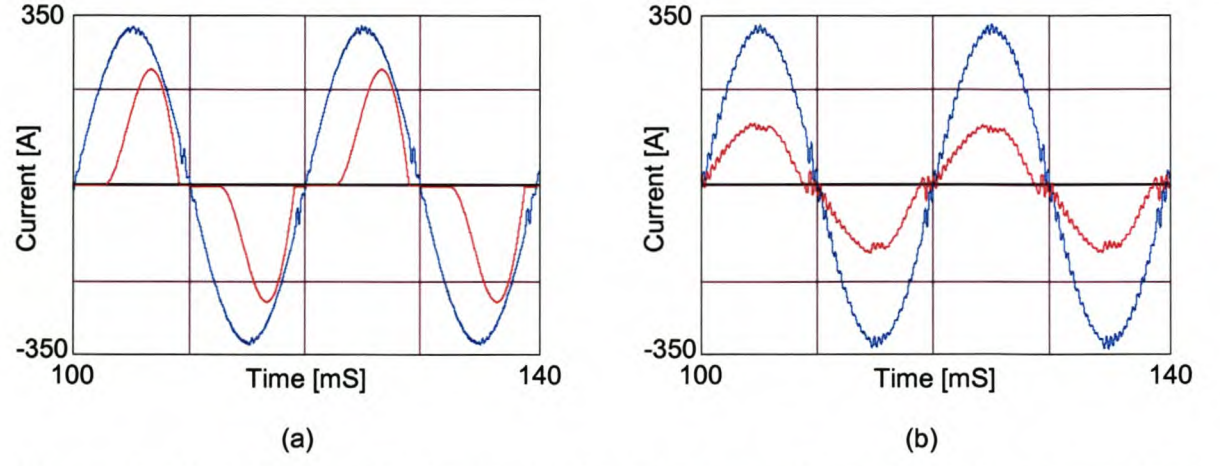


Figure 5-57 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace)

From the above simulation results can be seen that the shunt active power filter utilising the constant rate sliding mode current controller with time delay and dead-time compensation work satisfactorily.

5.6.7 Constant rate plus proportional current controller without the neutral inductor connected

Figure 5-58 (a) and Figure 5-58 (b) illustrate the phase A (blue trace), B (red trace), and C (green trace) load currents and the phase A (blue trace), B (red trace), and C (green trace) source currents after compensation respectively. The load currents produce a negative sequence unbalance of 50% and a zero sequence unbalance of 50%. After compensation the negative sequence unbalance is reduced to 1.9%, and the zero sequence unbalance is reduced to 2.0%. The phase A and B source currents have a TDD of 49.2% before compensation and after compensation the TDD for phase A is reduced to 6.2%, phase B to 6.5% and phase C to 1.9%.

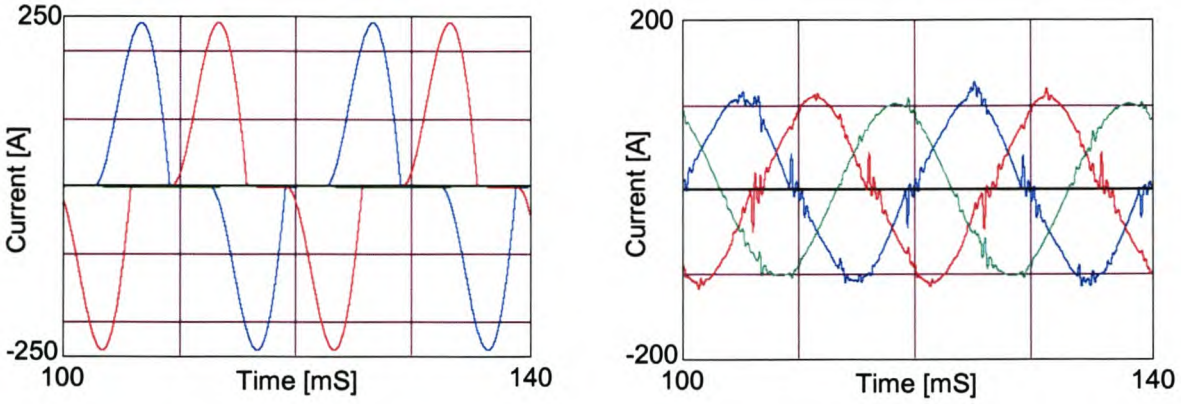


Figure 5-58 Simulation results showing (a) load current, and (b) compensated source currents

Figure 5-59 (a) shows the load current, and Figure 5-59 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 5-59 (c).

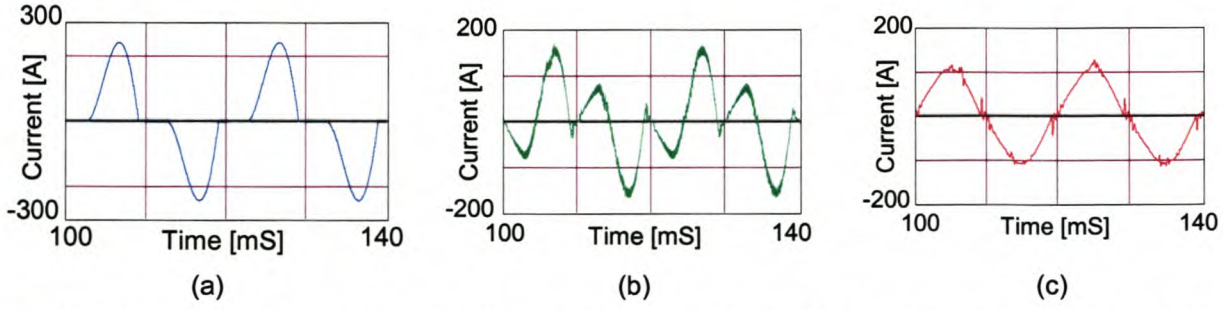


Figure 5-59 Simulation results showing Phase A (a) load current, (b) compensating current, and (c) compensated source current

Figure 5-60 (a) shows the uncompensated neutral current, and Figure 5-60 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 5-60 (c).

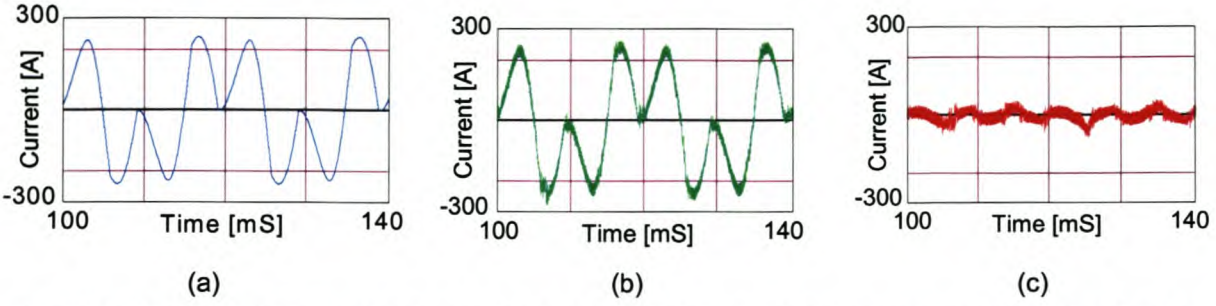


Figure 5-60 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 5-61 (a) and Figure 5-61 (b) shows the phase A source current and the phase A supply voltage before and after compensation respectively. From this it can be seen that reactive power compensation is achieved.

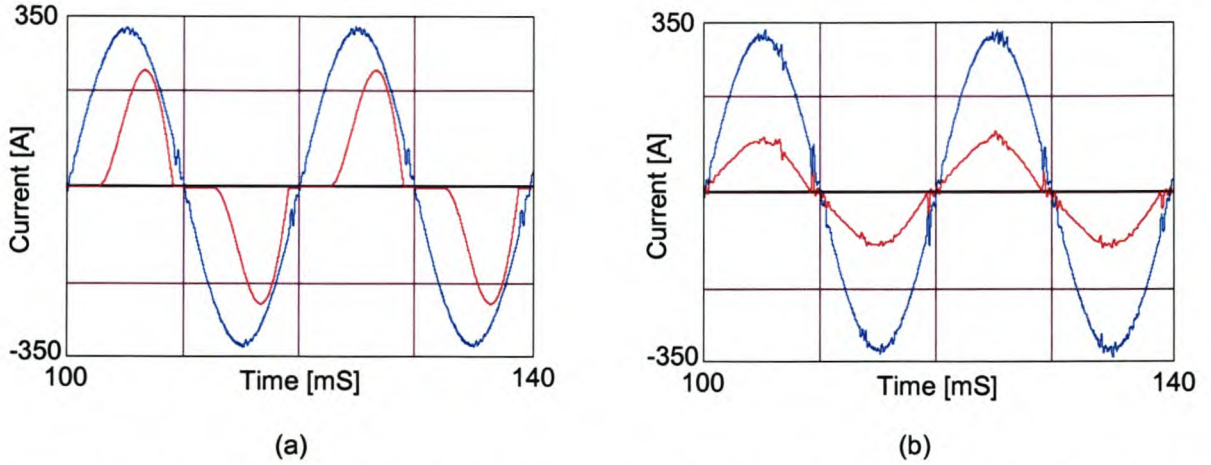


Figure 5-61 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace)

From the above simulation results can be seen that the shunt active power filter utilising the constant rate plus proportional sliding mode current controller with time delay and dead-time compensation work satisfactorily.

5.6.8 Constant rate plus proportional current controller with the neutral inductor connected

Figure 5-62 (a) and Figure 5-62 (b) illustrate the phase A (blue trace), B (red trace), and C (green trace) load currents and the phase A (blue trace), B (red trace), and C (green trace) source currents after compensation respectively. The load currents produce a negative sequence unbalance of 50% and a zero sequence unbalance of 50%. After compensation the negative sequence unbalance is reduced to 1.2%, and the zero sequence unbalance is reduced to 2.8%. The phase A and B source currents have a TDD of 49.2% before compensation and after compensation the TDD for phase A is reduced to 7.6%, phase B to 6.2% and phase C to 2.1%.

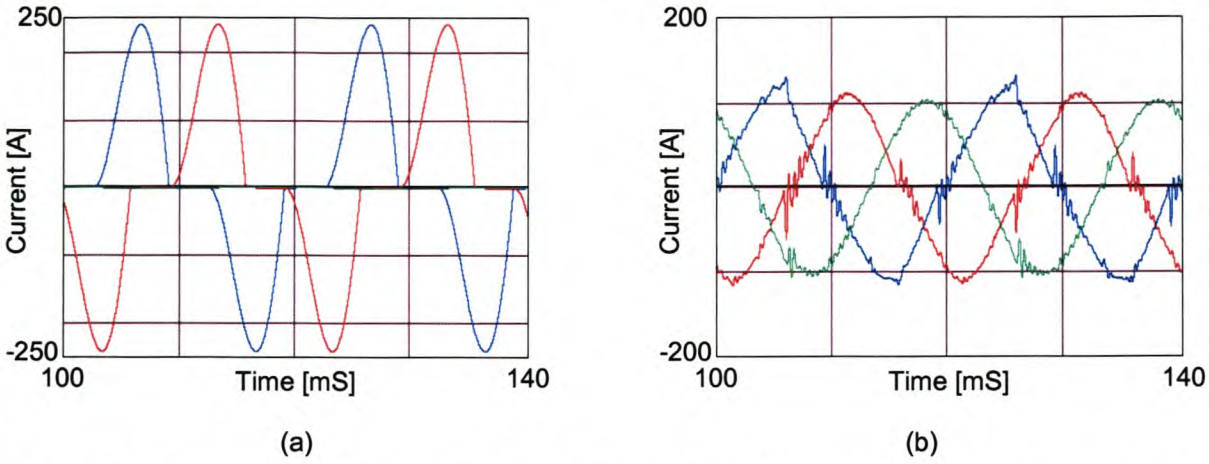


Figure 5-62 Simulation results showing (a) load current, and (b) compensated source currents

Figure 5-63 (a) shows the load current, and Figure 5-64 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 5-64 (c).

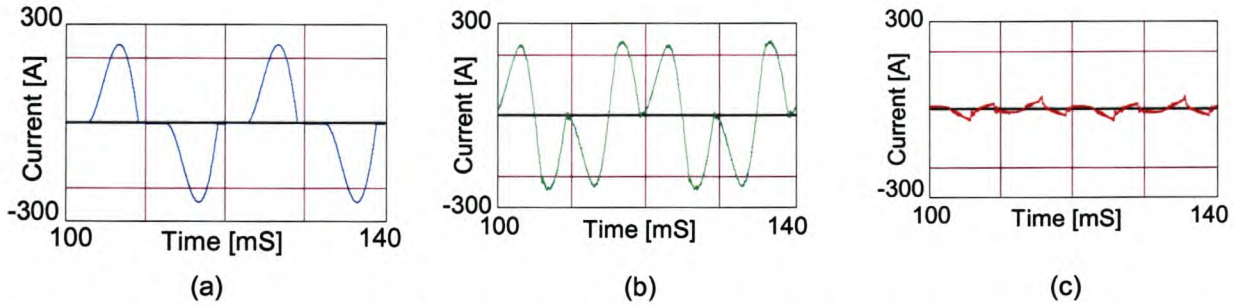


Figure 5-63 Simulation results showing Phase A (a) load current, (b) compensating current, and (c) compensated source current

Figure 5-64 (a) shows the uncompensated neutral current, and Figure 5-63 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 5-63 (c).

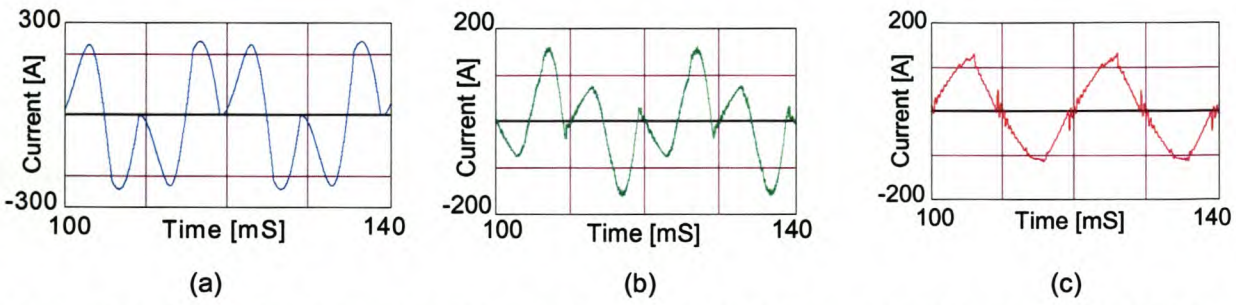


Figure 5-64 Simulation results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 5-65 (a) and Figure 5-65 (b) shows the phase A source current and the phase A supply voltage before and after compensation respectively. From this it can be seen that reactive power compensation is achieved.

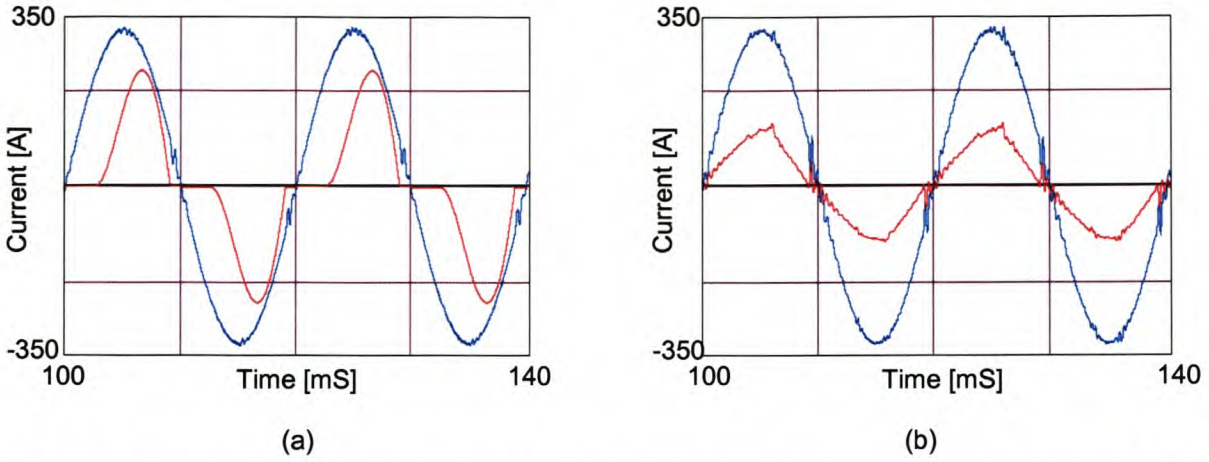


Figure 5-65 Simulation results showing (a) phase A voltage (blue trace) and load current (red trace), (b) phase A voltage (blue trace) and compensated source current (red trace)

From the above simulation results can be seen that the shunt active power filter utilising the constant rate plus proportional sliding mode current controller with time delay and dead-time compensation work satisfactorily.

5.7 Summary

This chapter dealt with the effects of when the current controllers are implemented practically. One of the practical issues that were addressed was the effect that the time delay have on the performance of a current-controlled voltage source inverter. A time delay compensation strategy was implemented and its operation was confirmed from the simulations. Additionally, the effect that dead-time has on the performance of a voltage source inverter was discussed in detail. Based on this discussion a dead-time compensation strategy was developed for three-phase four-wire voltage source inverters that take the effect of a current direction change during a switching cycle into account.

In Table 17 the rms current error values found from the difference between the reference current components and the actual current components is summarised. From Table 17 it can be seen that the rms current error values found from the difference between the reference current components and the actual current components is generally higher when the neutral inductor is not connected. An exception is the constant rate current controller because when the neutral inductor is connected the gain of the current controller is too low to achieve proper current regulation. It can also be seen from Table 17, as expected, that the rms current error is higher when only the time delay compensation is implemented.

Table 17 – Summary of the rms current error values

Type of control	Phase A [A]		Phase B [A]		Phase C [A]	
	Sinusoidal	Square	Sinusoidal	Square	Sinusoidal	Square
Predictive current control without any compensation (Without neutral inductor)	8.9	17.0	6.1	11.8	2.1	9.8
Predictive current control without any compensation (With neutral inductor)	6.0	14.0	4.6	11.8	3.7	8.6
Predictive current control with time delay compensation (Without neutral inductor)	16.0	17.7	9.9	13.1	3.6	11.5
Predictive current control with time delay compensation (With neutral inductor)	11.3	13.9	8.8	12.0	6.6	10.3
Predictive current control with time delay and dead-time compensation (Without neutral inductor)	2.9	11.1	1.6	7.7	1.1	4.8
Predictive current control with time delay and dead-time compensation (With neutral inductor)	2.8	10.5	1.8	8.1	1.0	5.6
Ideal saturating control with time delay and dead-time compensation (Without neutral inductor)	1.7	11.0	0.8	7.9	0.6	6.4
Ideal saturating control with time delay and dead-time compensation (With neutral inductor)	1.5	10.4	0.9	8.2	0.5	5.7
Constant rate control with time delay and dead-time compensation (Without neutral inductor)	1.6	9.8	0.8	7.8	0.7	5.6
Constant rate control with time delay and dead-time compensation (With neutral inductor)	1.6	15.0	1.0	8.9	0.8	5.7
Constant rate plus proportional control with time delay and dead-time compensation (Without neutral inductor)	1.7	11.3	1.1	8.5	0.7	7.5
Constant rate plus proportional control with time delay and dead-time compensation (With neutral inductor)	1.6	11.3	1.2	7.7	0.6	5.5

In Table 18 the TDD values for the respective phases is summarised, and in Table 19 the unbalance values for the respective phases is summarised.

When considering the average TDD and unbalance values it is found that the lowest average TDD and unbalance values is found when the ideal saturating current controller and the constant rate plus proportional current controller is implemented.

Table 18 – Summary of the TDD values for the different current controllers

Type of control	Phase A [%]	Phase B [%]	Phase C [%]
Predictive current control with time delay and dead-time compensation (Without neutral inductor)	10.1	11.0	1.4
Predictive current control with time delay and dead-time compensation (With neutral inductor)	10.9	11.1	1.2
Ideal saturating control with time delay and dead-time compensation (Without neutral inductor)	5.6	6.7	1.7
Ideal saturating control with time delay and dead-time compensation (With neutral inductor)	6.7	6.4	1.6
Constant rate control with time delay and dead-time compensation (Without neutral inductor)	10.5	9.5	3.8
Constant rate control with time delay and dead-time compensation (With neutral inductor)	13.2	10.9	5.1
Constant rate plus proportional control with time delay and dead-time compensation (Without neutral inductor)	6.2	6.5	1.9
Constant rate plus proportional control with time delay and dead-time compensation (With neutral inductor)	7.6	6.2	2.1

Table 19 – Summary of the unbalance values for the different current controllers

Type of control	Negative sequence unbalance [%]	Zero sequence unbalance [%]
Predictive current control with time delay and dead-time compensation (Without neutral inductor)	3.7	3.1
Predictive current control with time delay and dead-time compensation (With neutral inductor)	3.3	3.6
Ideal saturating control with time delay and dead-time compensation (Without neutral inductor)	2.1	1.7
Ideal saturating control with time delay and dead-time compensation (With neutral inductor)	1.5	2.2
Constant rate control with time delay and dead-time compensation (Without neutral inductor)	0.8	3.3
Constant rate control with time delay and dead-time compensation (With neutral inductor)	2.1	2.8
Constant rate plus proportional control with time delay and dead-time compensation (Without neutral inductor)	1.9	2.0
Constant rate plus proportional control with time delay and dead-time compensation (With neutral inductor)	1.2	2.8

From this results it can be seen that the current controllers that have the best performance is respectively the ideal saturating current controller and the constant rate plus proportional current controller when the TDD distortion values is considered.

In Chapter 6 the discussed theory will be implemented practically to validate the performance of the different current controllers.

6. Practical results of theory presented

6.1 Introduction

This chapter will provide practical results of the discussed theory.

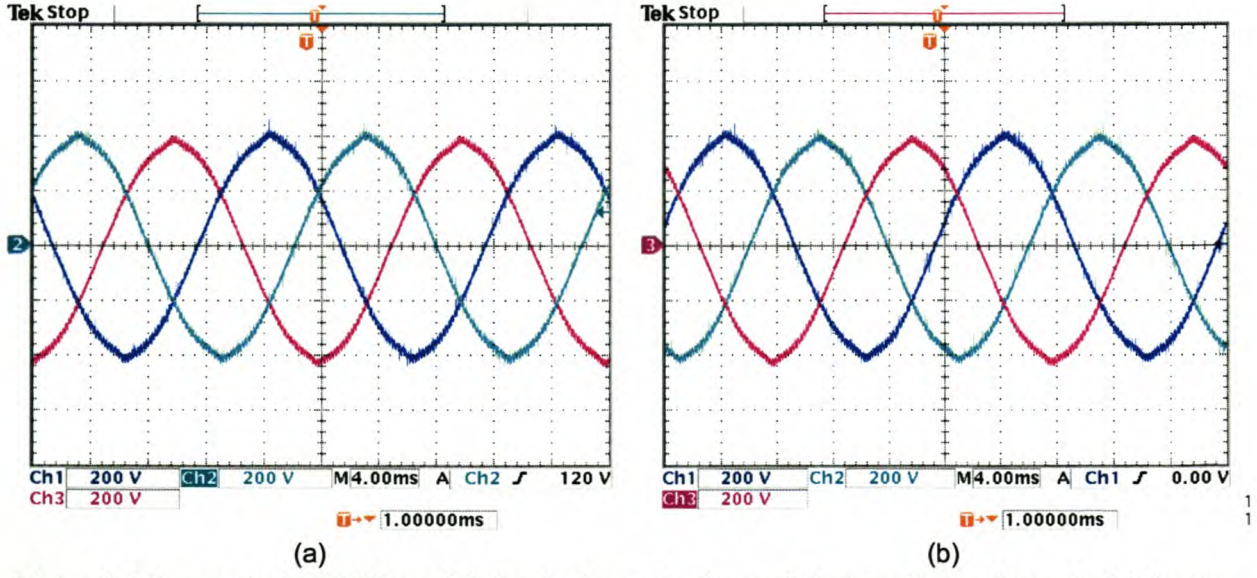
First the performance of the three-dimensional space vector PWM technique will be evaluated. The practical setup used for evaluating the performance of the three-dimensional space vector PWM technique is shown in Appendix C-3, and the practical setup used to evaluate the current controllers performance is described in Appendix C-1. The reference current components used to evaluate the performance of the current controllers are the same as was used in Chapter 4. It must be noted that the actual current waveforms in Section 6.3 is labelled in the following manner; phase A - Channel 1, phase B - Channel 2, and phase C - Channel 3.

Finally the shunt active power filter performance will be validated through practical results in Section 6.4, utilising the setup as shown in Appendix C-2.

6.2 Space vector PWM

In this section the working of the three-dimensional space vector PWM modulating technique is illustrated.

Figure 6-1 (a) shows the currently implemented space vector modulating scheme open loop output voltages when balanced three-phase voltages is applied as references, and in Figure 6-1 (b) the new three-dimensional space vector modulating algorithm is used to modulate the same output reference voltages.

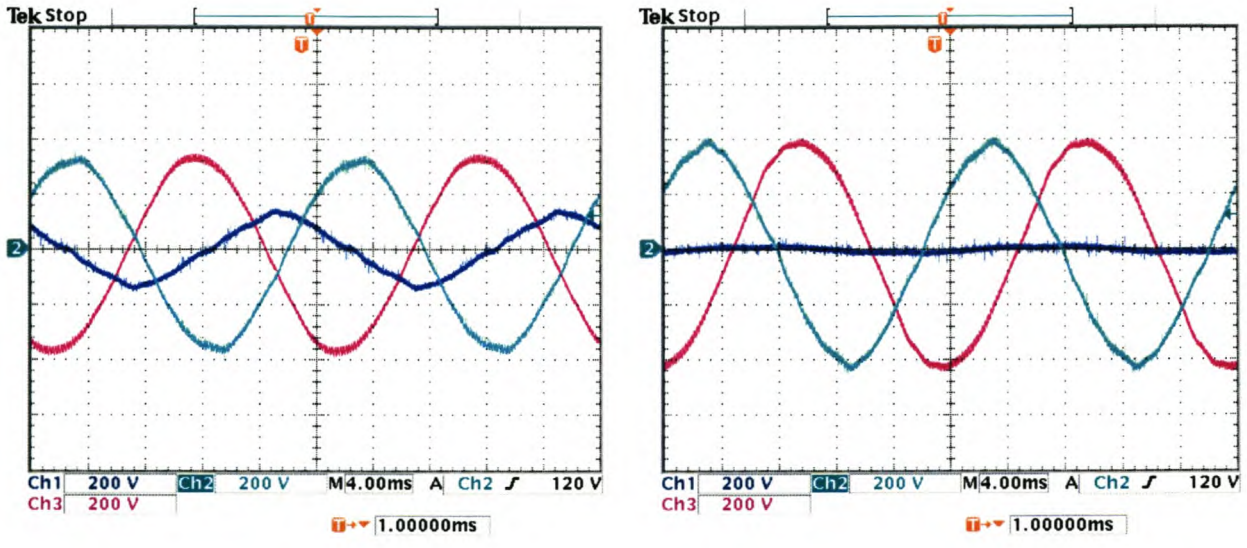


(a) (b)

Figure 6-1 Space vector PWM modulating balanced voltages (a) currently implemented, (b) new three-dimensional space vector PWM

In order to generate unbalanced currents the inverter must be able to modulate unbalanced voltages. Figure 6-2 (a) shows the currently implemented space vector modulating scheme open loop output

voltages when unbalanced three-phase voltages is applied as references, and in Figure 6-2 (b) the new three-dimensional space vector modulating algorithm is used to modulate the unbalnced output reference voltages. Unbalanced voltages was generated by forcing one phase voltage to be zero.



(a) (b)

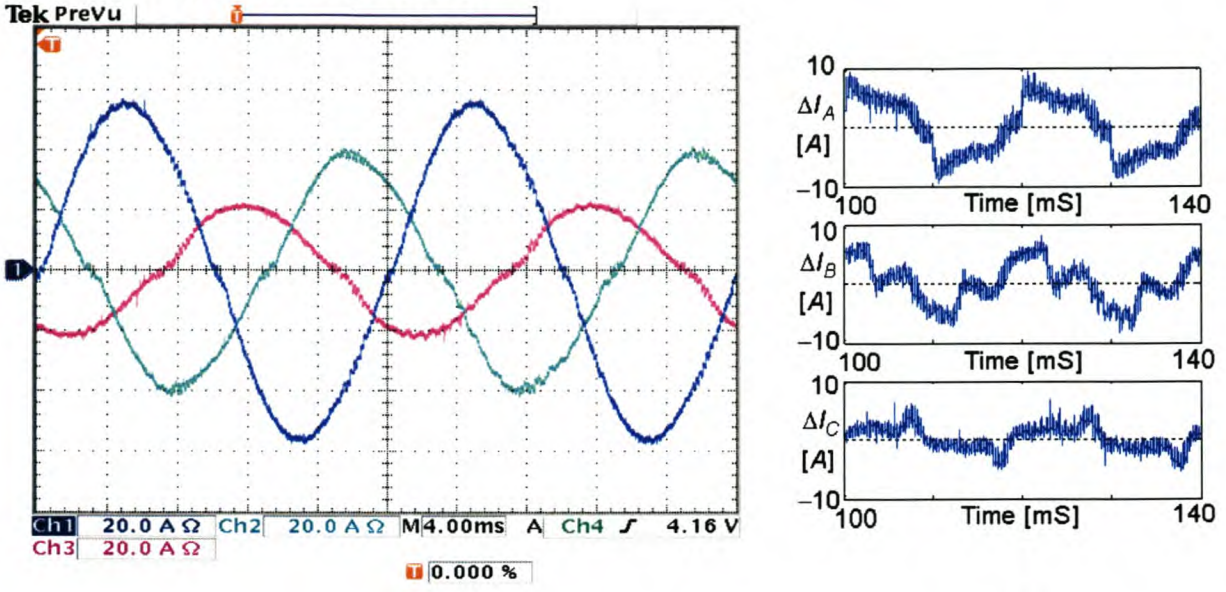
Figure 6-2 Space vector PWM modulating unbalanced voltages (a) currently implemented, (b) new three-dimensional space vector PWM

As can be seen from the above figures the three-dimensional modulating strategy's ability to generate unbalanced voltages is superior to the space vector-modulating scheme that is currently implemented in the QUPS.

6.3 Current regulation

This section will confirm the performance of the simulated current controllers, as shown in Chapter 5, practically.

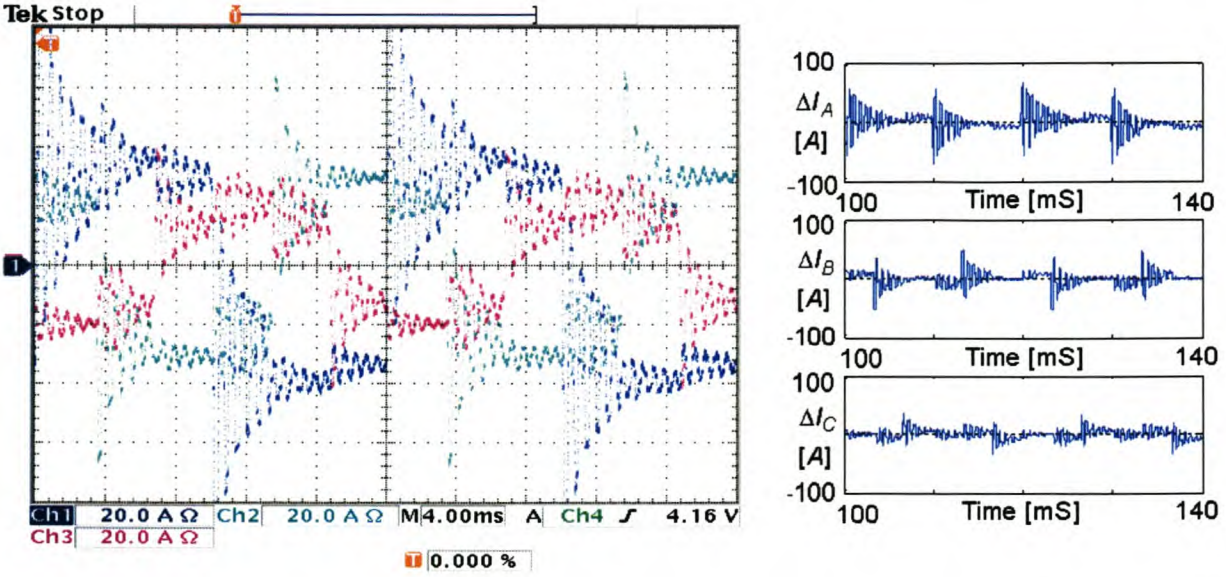
6.3.1 Predictive current control



(a) (b)

Figure 6-3 Predictive current controller without neutral inductor connected, using sinusoidal references, with no time delay compensation implemented.

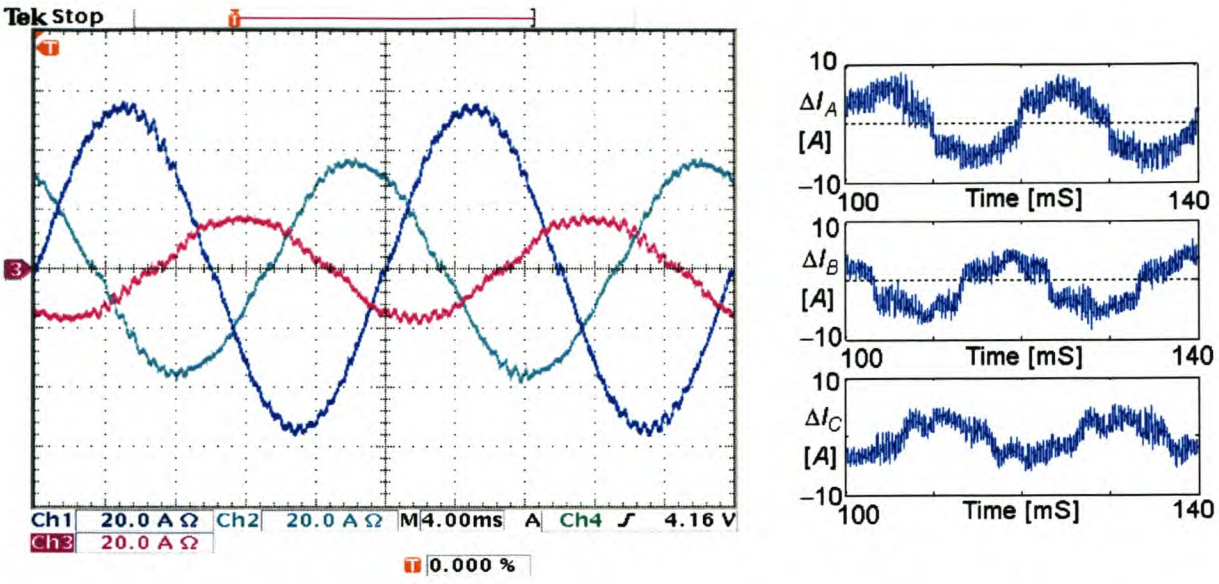
Figure 6-3 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 4.5 A, 3.4 A and 2.0 A respectively.



(a) (b)

Figure 6-4 Predictive current controller without neutral inductor connected, using square references, with no time delay compensation implemented.

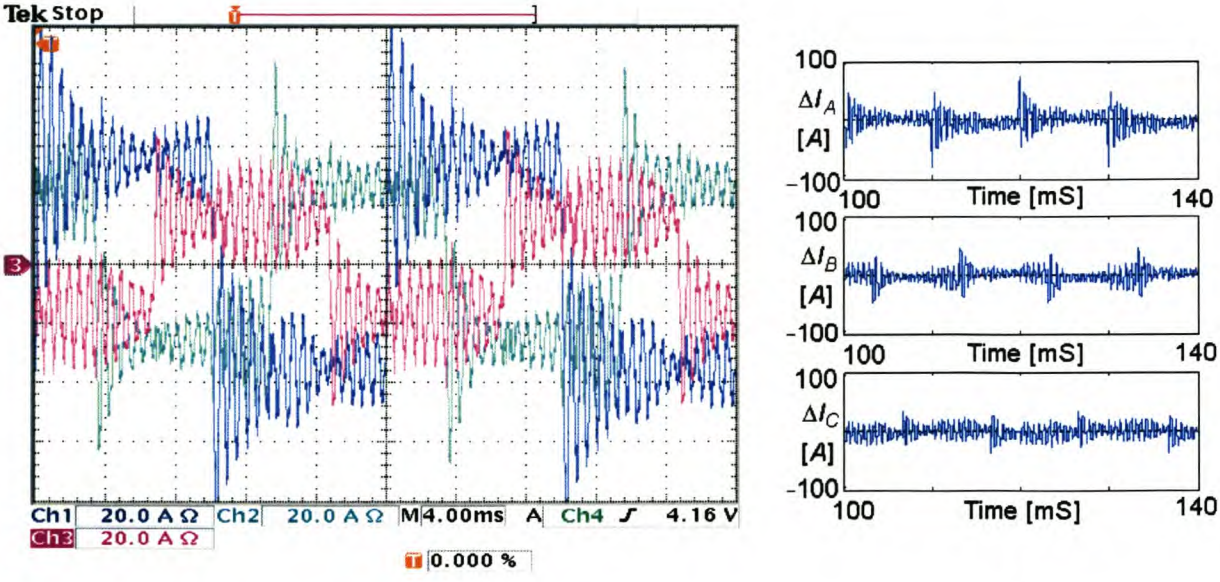
Figure 6-4 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 17.0 A, 11.5 A and 8.6 A respectively.



(a) (b)

Figure 6-5 Predictive current controller with neutral inductor connected, using sinusoidal references, with no time delay compensation implemented.

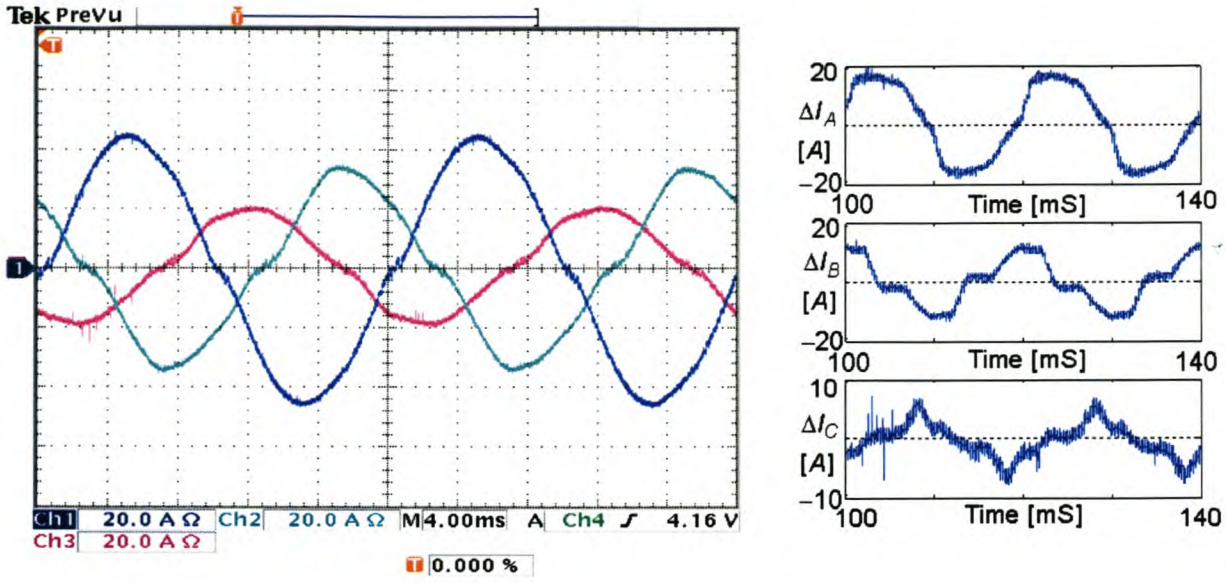
Figure 6-5 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 4.3 A, 3.4 A and 2.5 A respectively.



(a) (b)

Figure 6-6 Predictive current controller with neutral inductor connected, using square references, with no time delay compensation implemented.

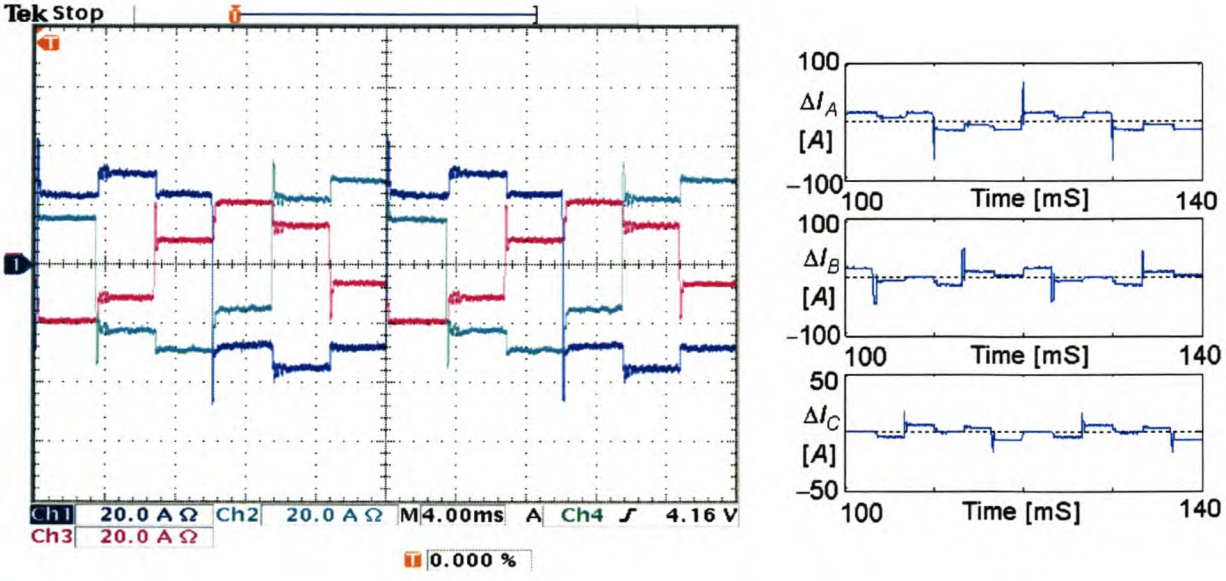
Figure 6-6 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 15.0 A, 11.4 A and 11.0 A respectively.



(a) (b)

Figure 6-7 Predictive current controller without neutral inductor connected, using sinusoidal references, with time delay compensation implemented.

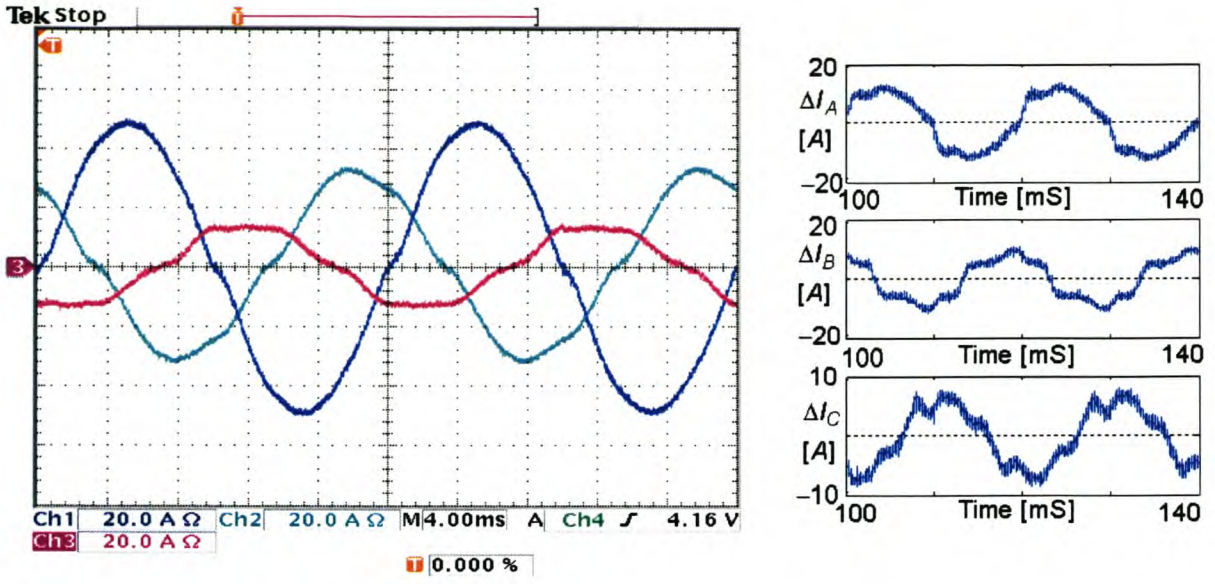
Figure 6-7 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 12.5 A, 7.6 A and 2.8 A respectively.



(a) (b)

Figure 6-8 Predictive current controller without neutral inductor connected, using square references, with time delay compensation implemented.

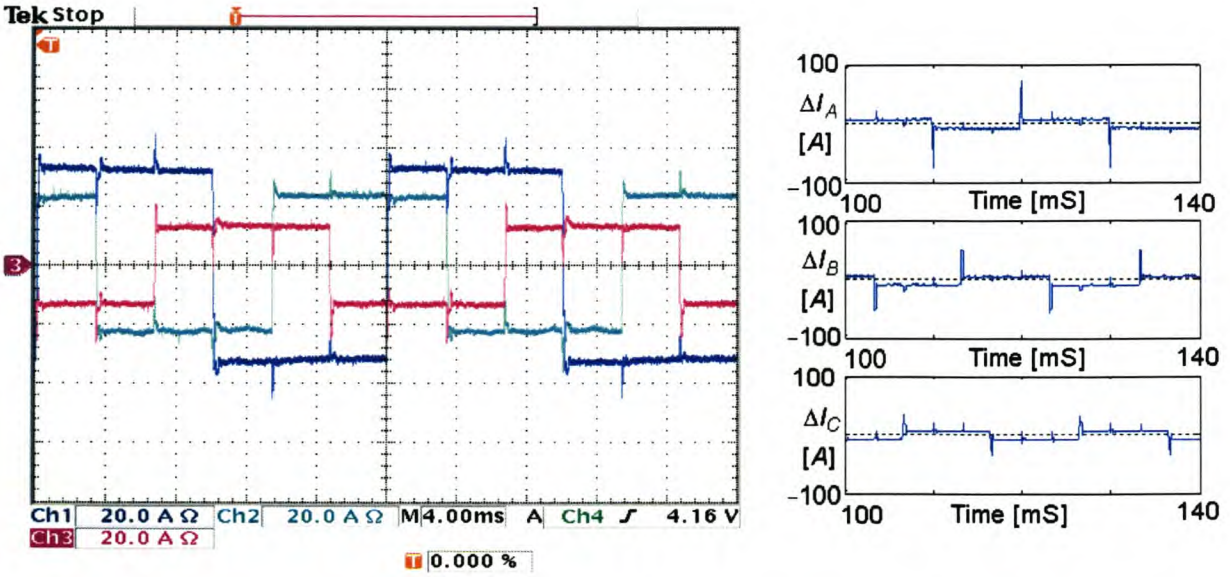
Figure 6-8 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 13.6 A, 10.8 A and 9.2 A respectively.



(a) (b)

Figure 6-9 Predictive current controller with neutral inductor connected, using sinusoidal references, with no time delay compensation implemented.

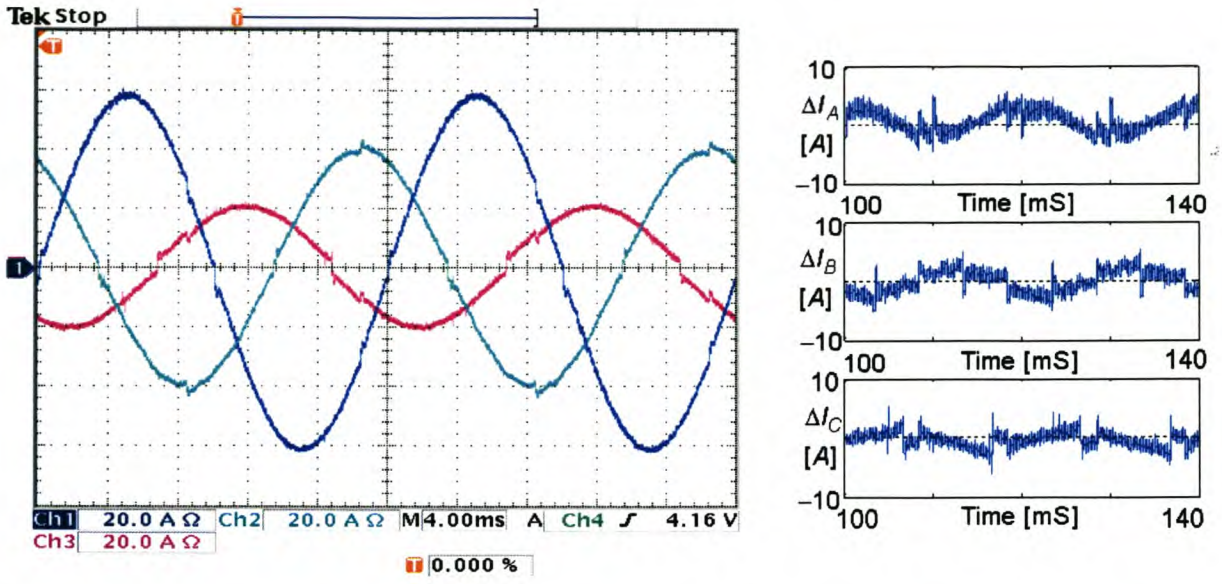
Figure 6-9 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 8.7 A, 6.6 A and 4.7 A respectively.



(a) (b)

Figure 6-10 Predictive current controller with neutral inductor connected, using square references, with time delay compensation implemented.

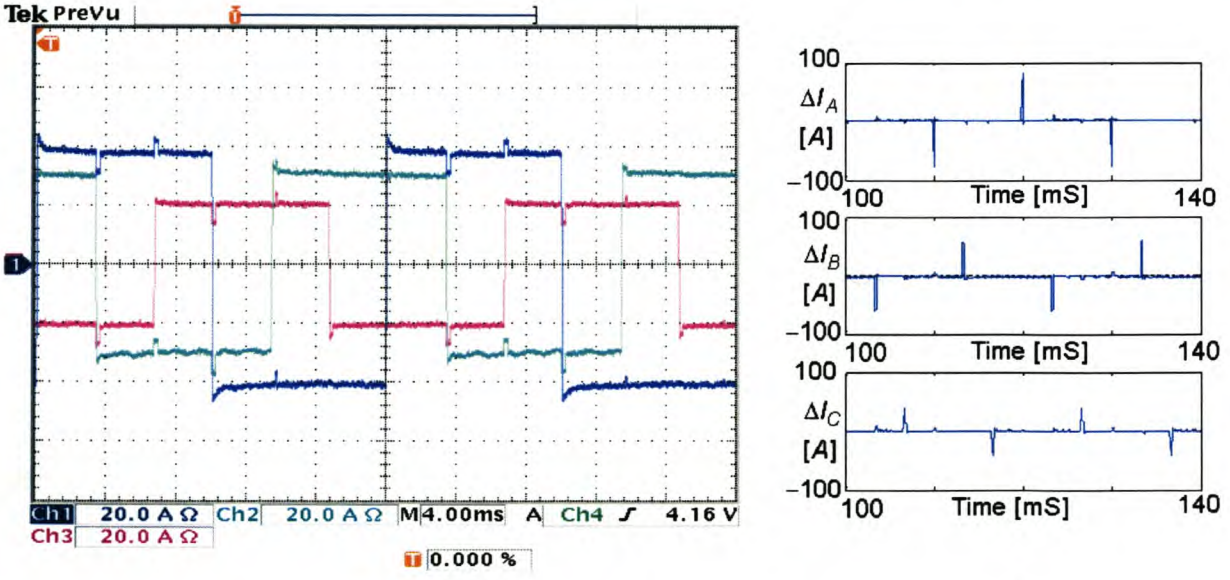
Figure 6-10 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 10.5 A, 9.6 A and 7.7 A respectively.



(a) (b)

Figure 6-11 Predictive current controller without neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented.

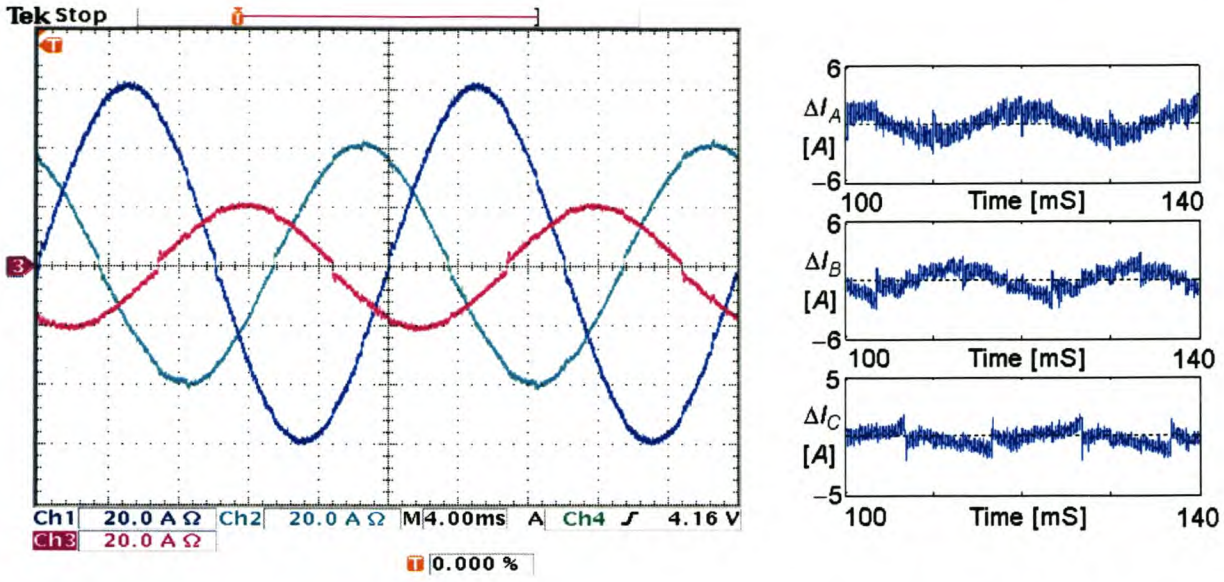
Figure 6-11 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 1.7 A, 1.7 A and 1.2 A respectively.



(a) (b)

Figure 6-12 Predictive current controller without neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented.

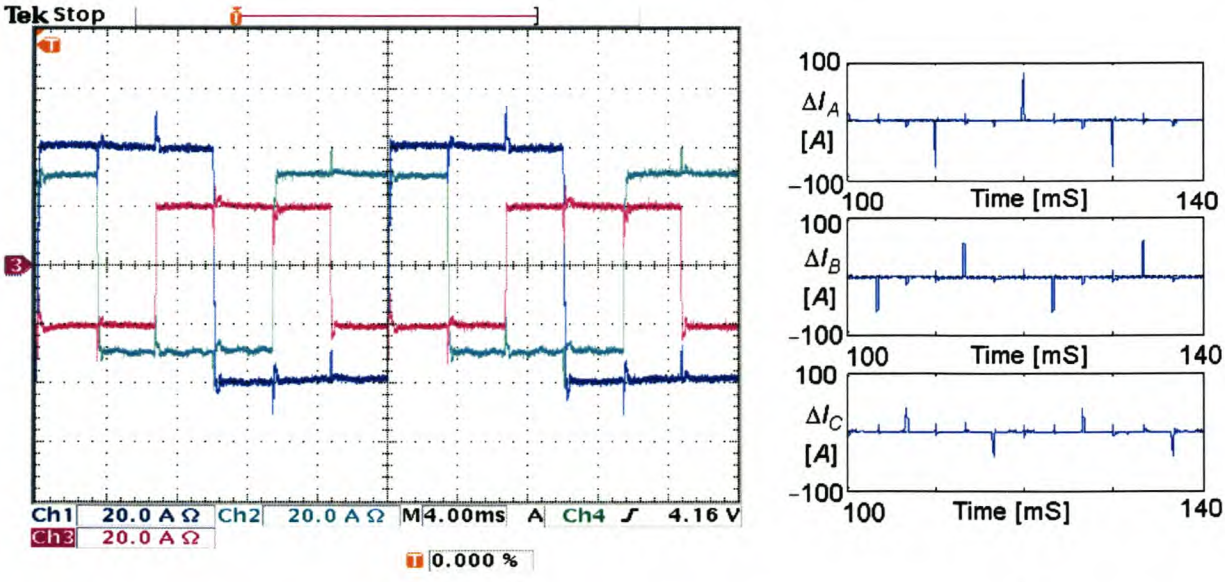
Figure 6-12 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 7.4 A, 7.6 A and 4.7 A respectively.



(a) (b)

Figure 6-13 Predictive current controller with neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented.

Figure 6-13 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 1.6 A, 1.5 A and 1.0 A respectively.

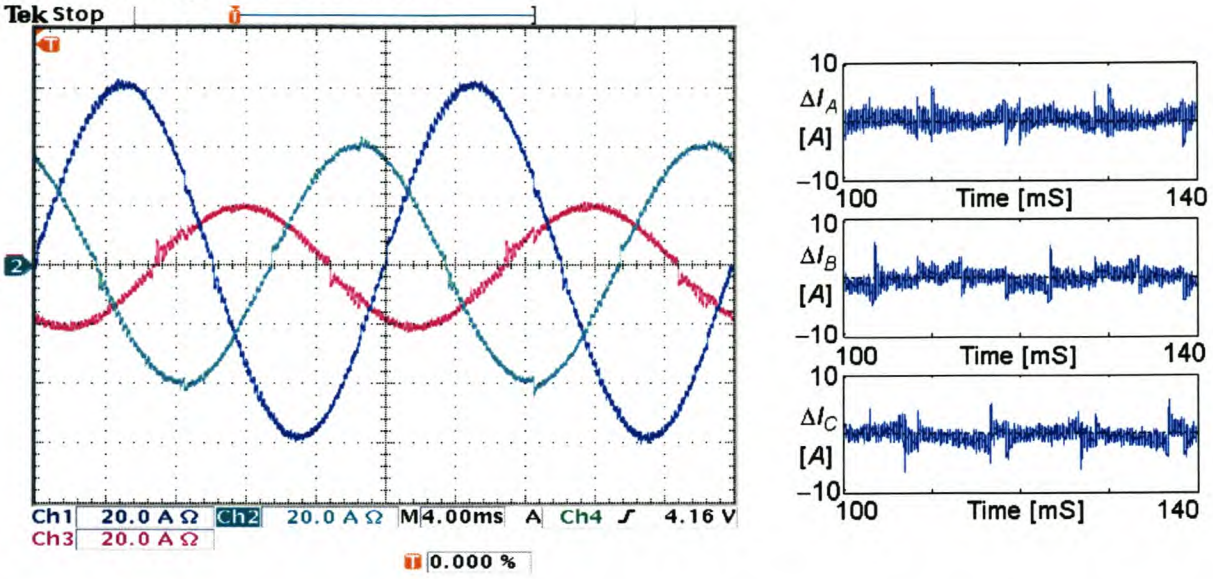


(a) (b)

Figure 6-14 Predictive current controller with neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented.

Figure 6-14 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 8.1 A, 7.5 A and 4.6 A respectively.

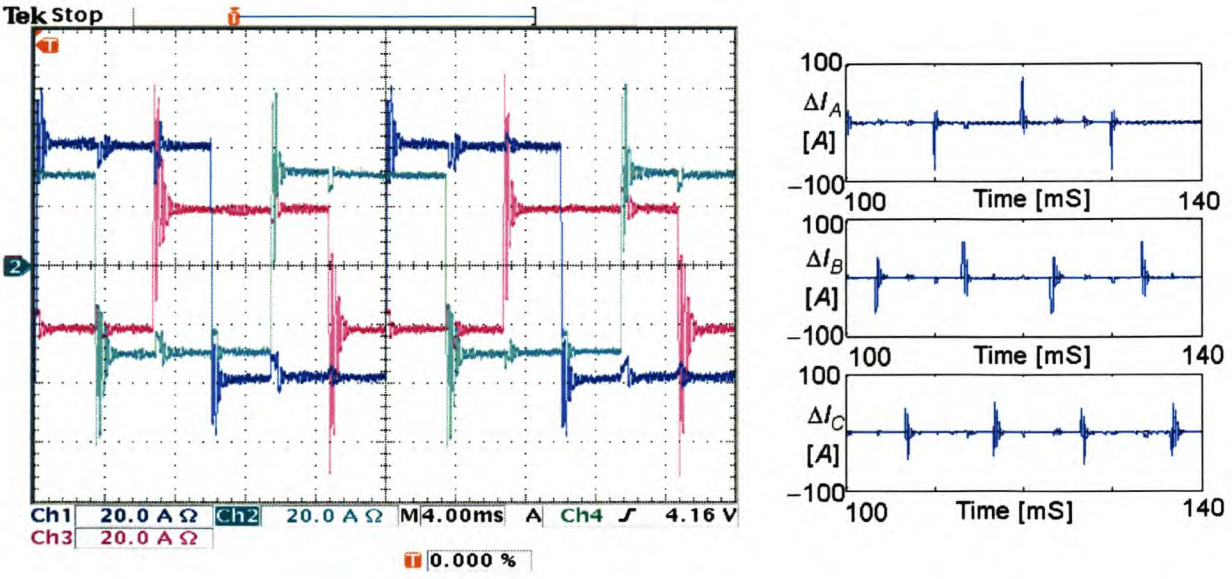
6.3.2 Sliding mode controllers



(a) (b)

Figure 6-15 Ideal saturation controller without the neutral inductor connected, using sinusoidal references, with time delay compensation and dead-time compensation implemented.

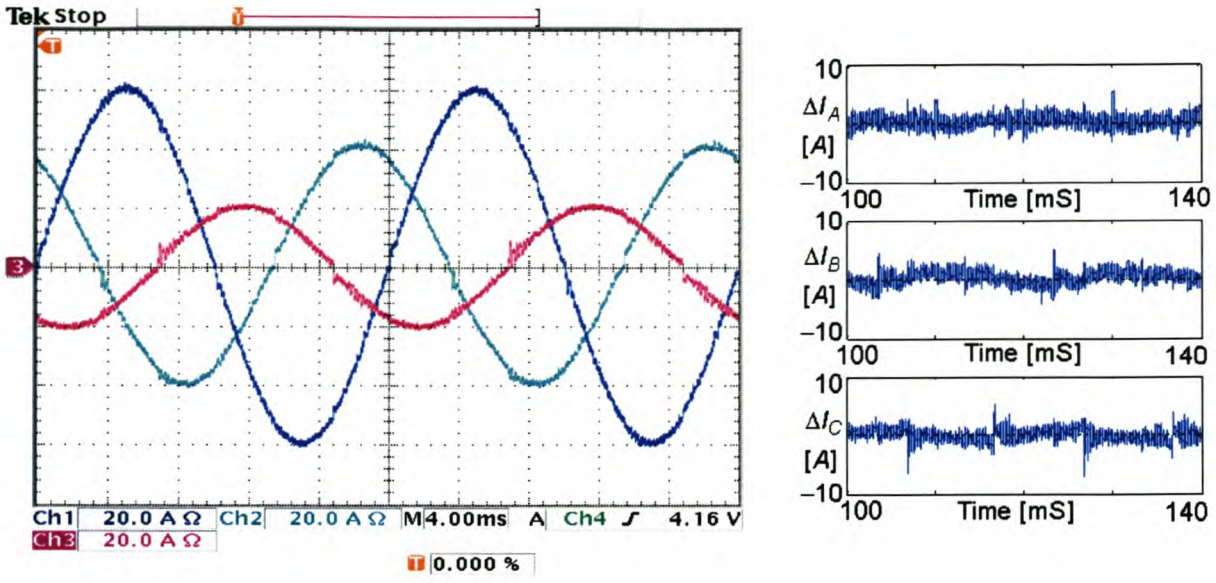
Figure 6-15 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 0.6 A, 1.0 A and 0.9 A respectively.



(a) (b)

Figure 6-16 Ideal saturation controller without the neutral inductor connected, using square references, with time delay compensation and dead-time compensation implemented.

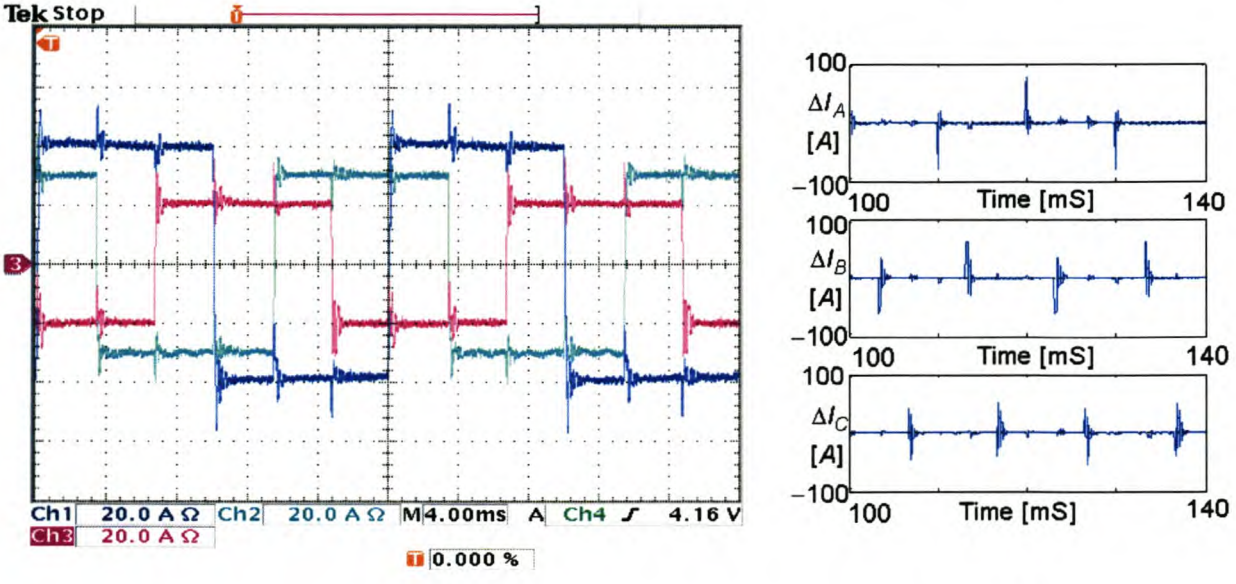
Figure 6-16 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 7.6 A, 8.0 A and 6.2 A respectively.



(a) (b)

Figure 6-17 Ideal saturation controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented.

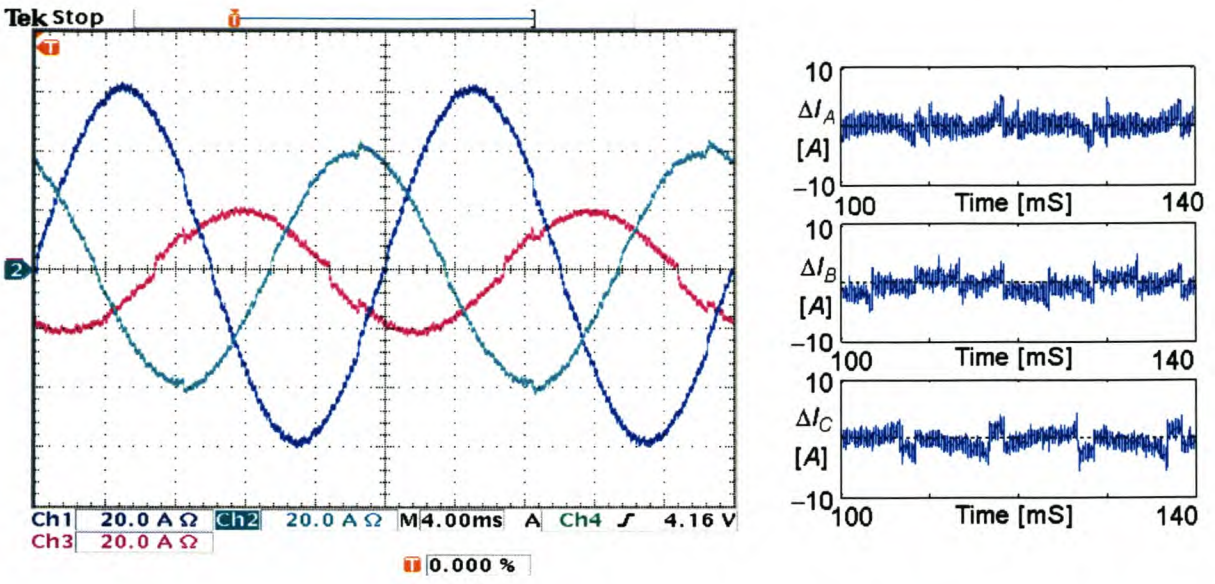
Figure 6-17 (b) show plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current error for phase A, phase B and phase C are 0.5 A, 0.8 A and 0.7 A respectively.



(a) (b)

Figure 6-18 Ideal saturation controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented.

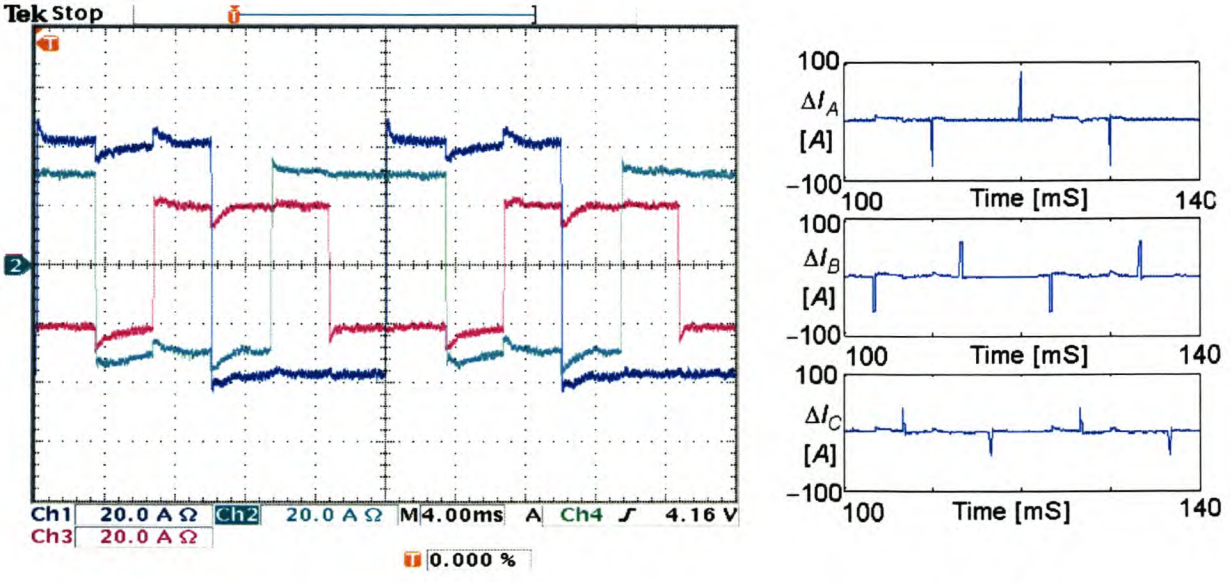
Figure 6-18 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 8.4 A, 7.8 A and 4.7 A respectively.



(a) (b)

Figure 6-19 Constant rate controller without the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented.

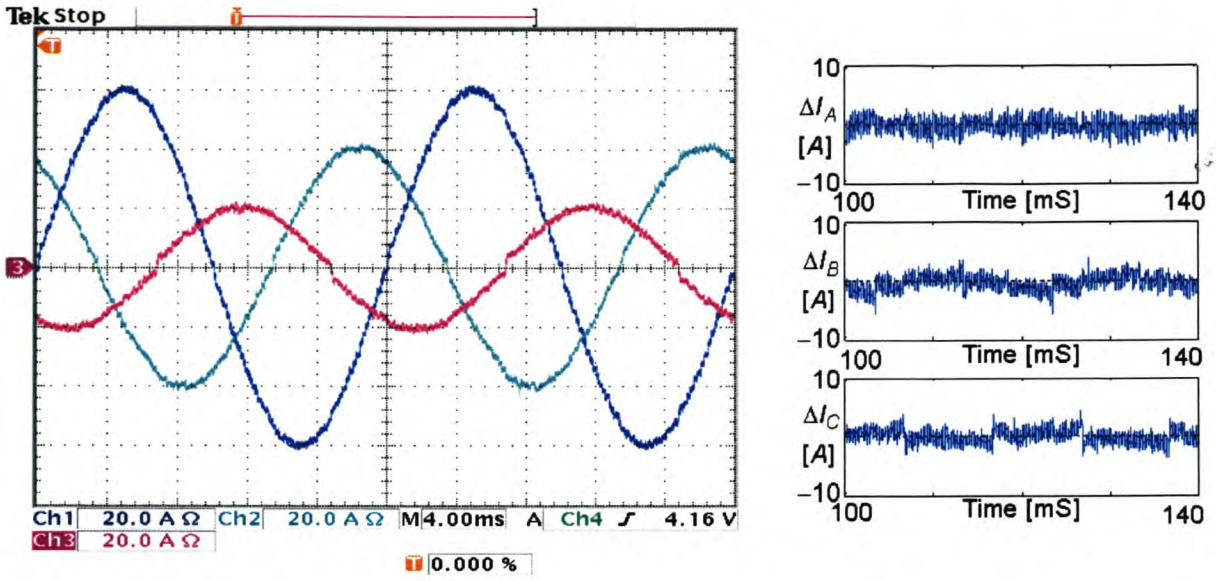
Figure 6-19 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 0.8 A, 1.2 A and 1.1 A respectively.



(a) (b)

Figure 6-20 Constant rate controller without the neutral inductor connected, using square references, with time delay and dead-time compensation implemented.

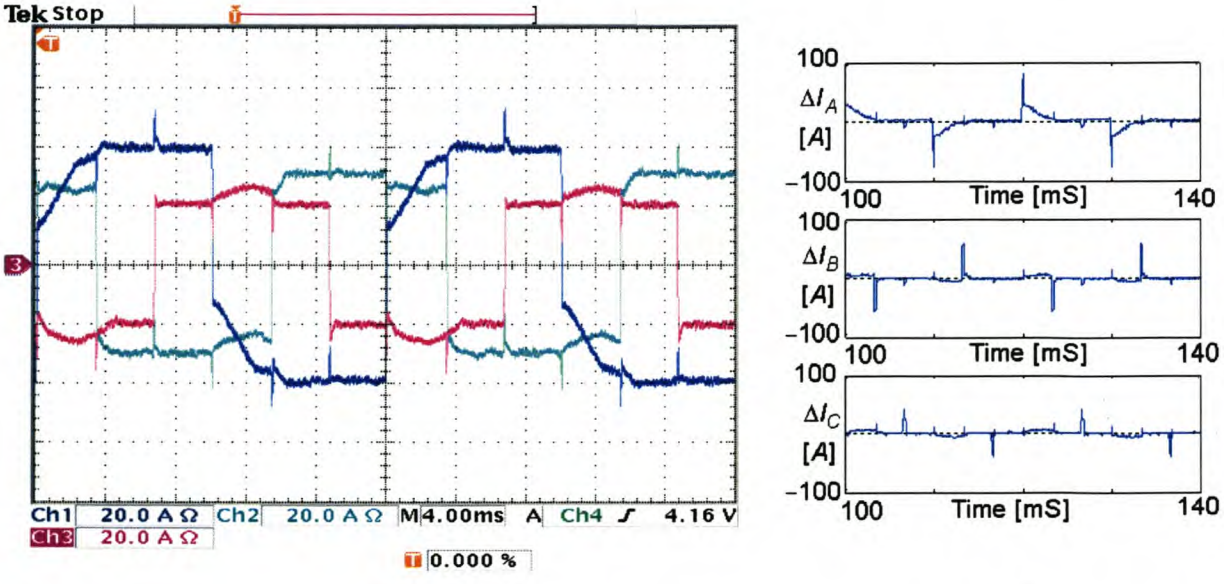
Figure 6-20 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 7.4 A, 7.7 A and 4.9 A respectively.



(a) (b)

Figure 6-21 Constant rate controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented.

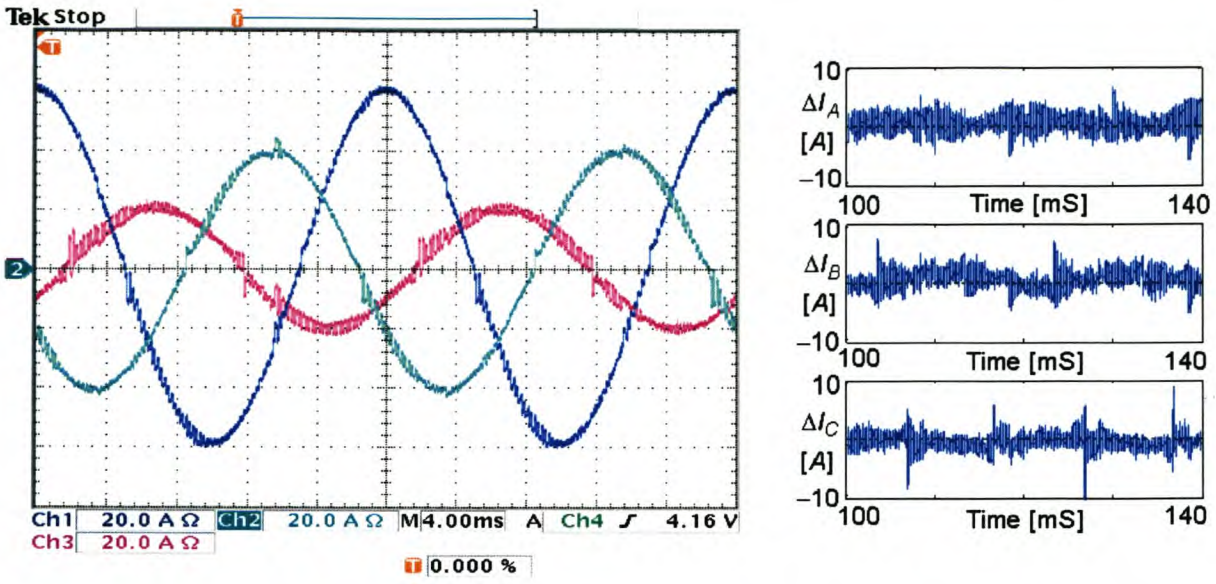
Figure 6-21 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 0.6 A, 0.9 A and 0.8 A respectively.



(a) (b)

Figure 6-22 Constant rate controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented.

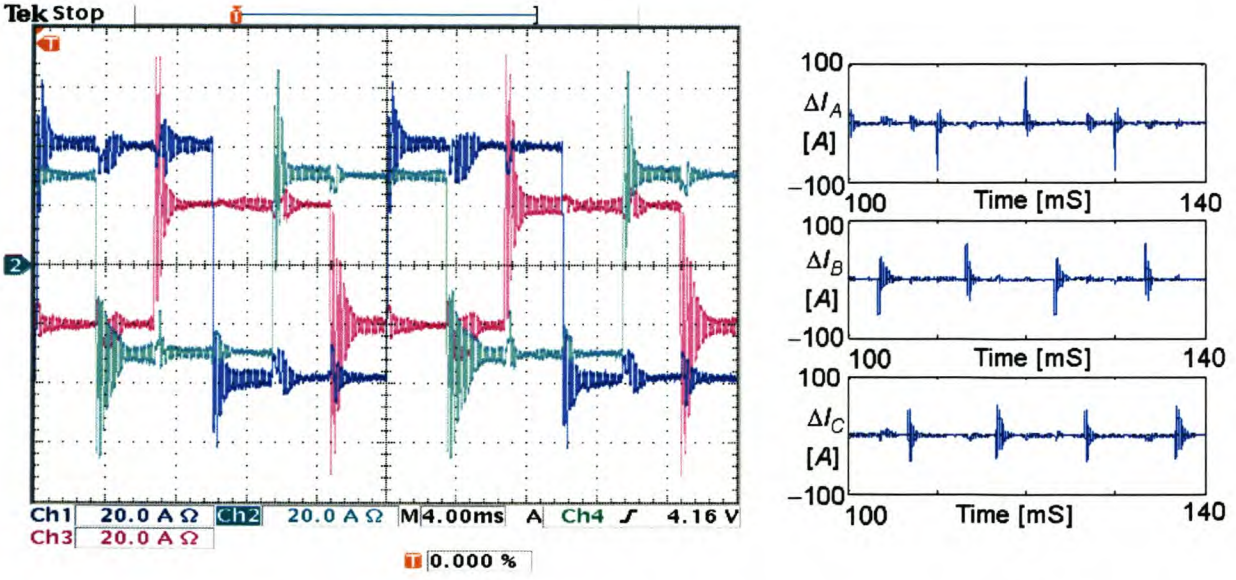
Figure 6-22 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 11.9 A, 7.6 A and 5.3 A respectively.



(a) (b)

Figure 6-23 Constant rate plus proportional controller without the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented.

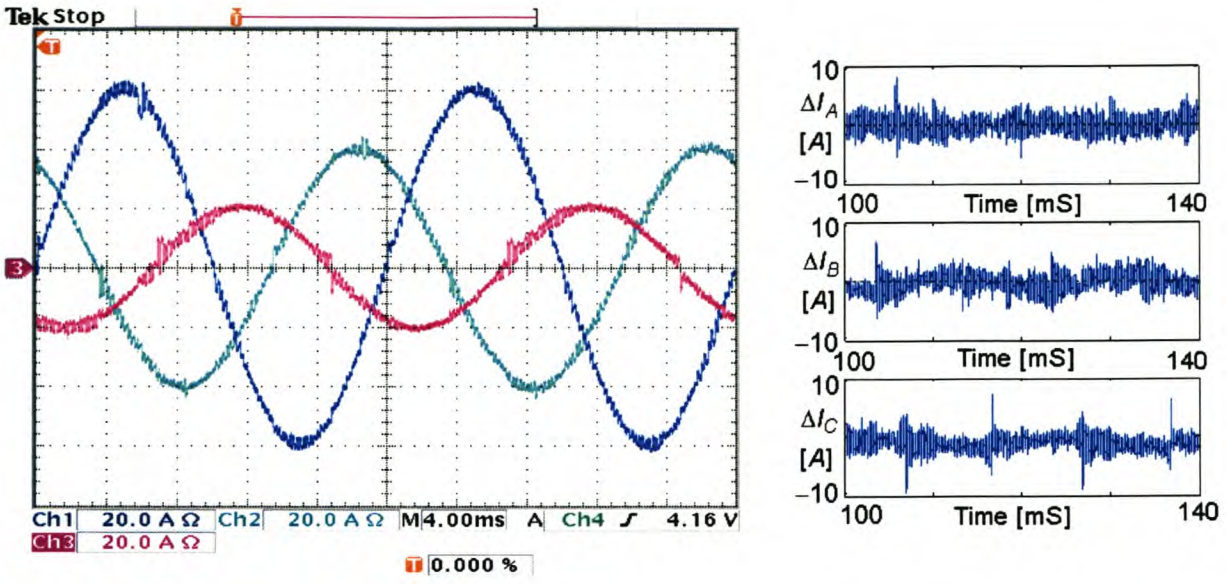
Figure 6-23 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 0.6 A, 0.9 A and 0.8 A respectively.



(a) (b)

Figure 6-24 Constant rate plus proportional controller without the neutral inductor connected, using square references, with time delay and dead-time compensation implemented.

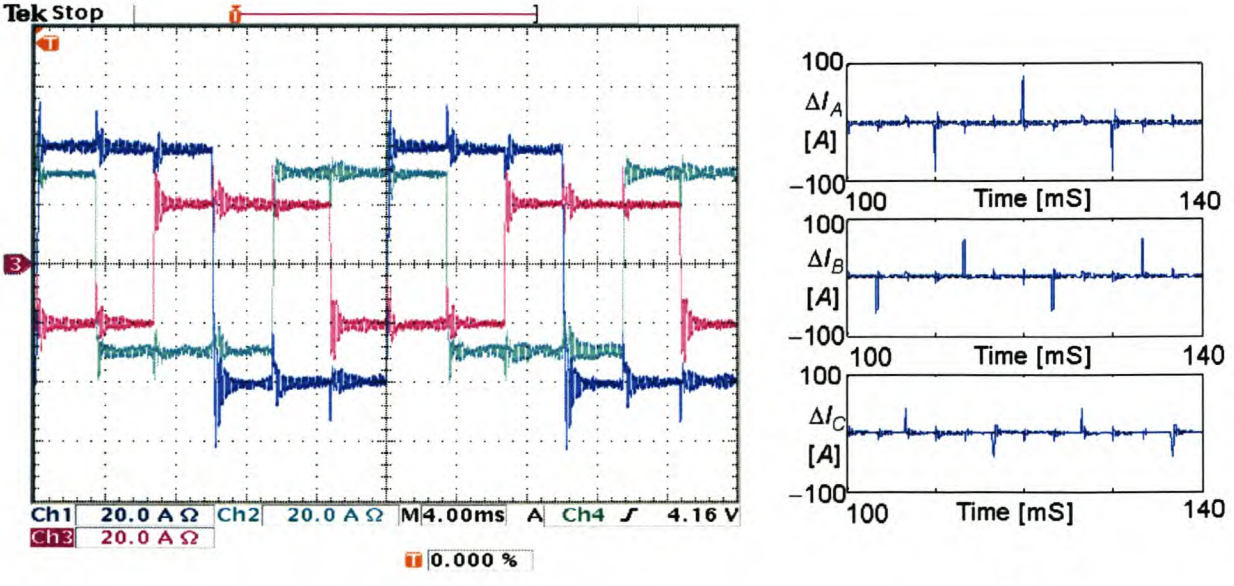
Figure 6-24 (b) show plots of the current errors between the square reference currents and the actual current waveforms when the neutral inductor is not connected. The rms current errors for phase A, phase B and phase C are 8.0 A, 8.5 A and 6.8 A respectively.



(a) (b)

Figure 6-25 Constant rate plus proportional controller with the neutral inductor connected, using sinusoidal references, with time delay and dead-time compensation implemented.

Figure 6-25 (b) shows plots of the current error between the sinusoidal reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 0.8 A, 0.9 A and 0.7 A respectively.



(a) (b)

Figure 6-26 Constant rate plus proportional controller with the neutral inductor connected, using square references, with time delay and dead-time compensation implemented.

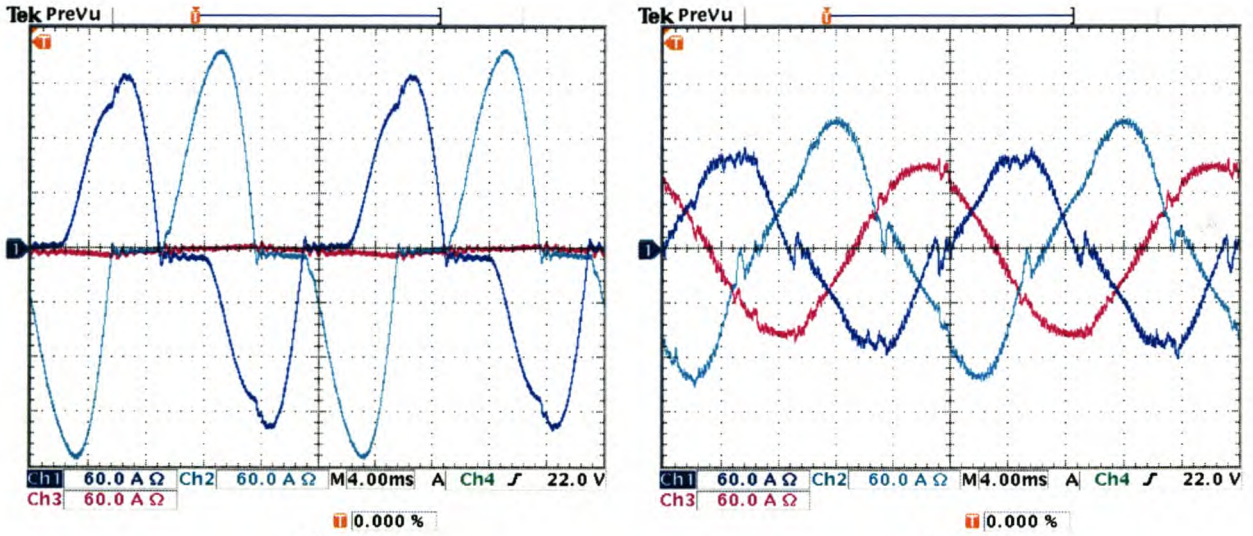
Figure 6-26 (b) shows plots of the current error between the square reference currents and the actual current waveforms when the neutral inductor is connected. The rms current errors for phase A, phase B and phase C are 8.2 A, 7.7 A and 4.7 A respectively.

6.4 Shunt Active power filtering

This section will implement practically the discussed current controllers in a shunt active power filter application. The extended synchronous reference frame technique discussed in Chapter 3 will be used to generate the reference current signals.

6.4.1 Predictive current controller – without neutral inductor

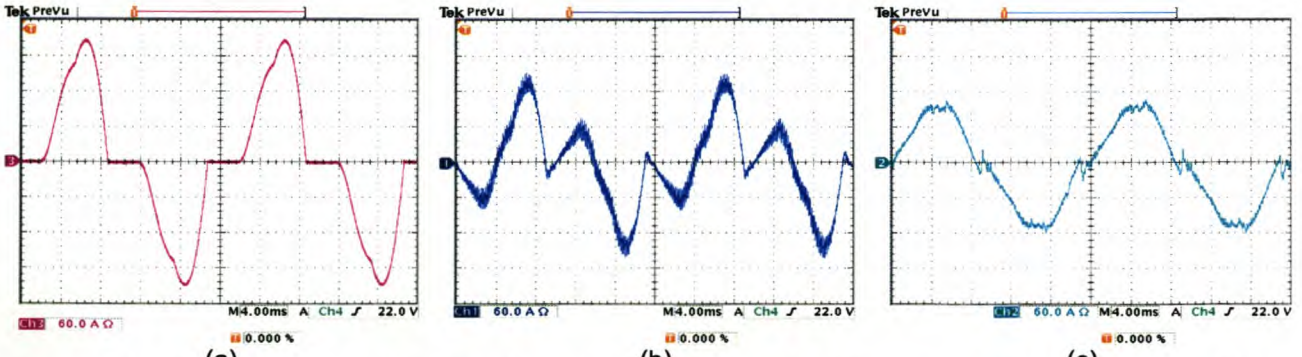
Figure 6-27 (a) and Figure 6-27 (b) illustrate the phase A (Channel 1), B (Channel 2), and C (Channel 3) load currents and the phase A, B and C source currents after compensation respectively. The load currents produce a negative sequence unbalance of 53.2% and a zero sequence unbalance of 48.0%. After compensation the negative sequence unbalance is reduced to 12.1%, and the zero sequence unbalance is reduced to 7.6%. The phase A and B source currents before compensation have a TDD of 35.4% and 44.0% respectively, and after compensation the TDD for phase A is reduced to 10.3%, phase B to 14.0% and phase C to 3.1%.



(a) (b)

Figure 6-27 Practical results showing (a) load current, and (b) compensated source currents

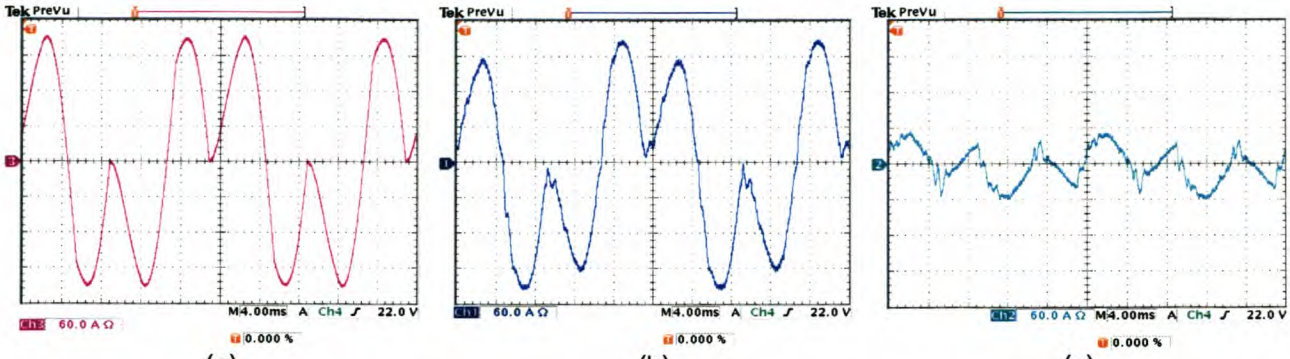
Figure 6-28 (a) shows the load current, and Figure 6-28 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 6-28 (c).



(a) (b) (c)

Figure 6-28 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

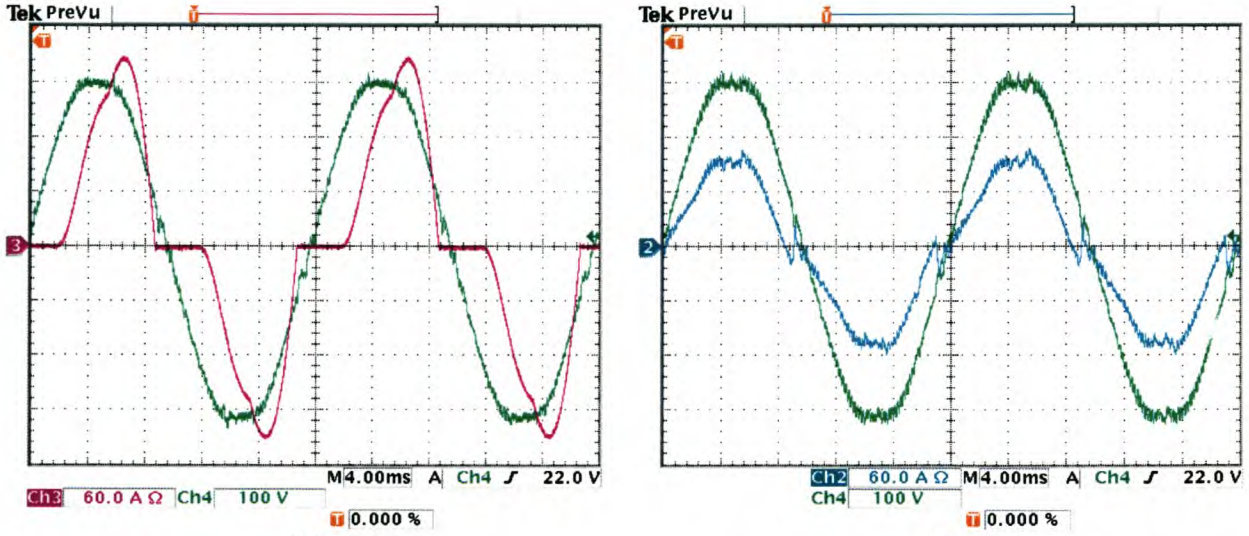
Figure 6-29 (a) shows the uncompensated neutral current, and Figure 6-29 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 6-29 (c).



(a) (b) (c)

Figure 6-29 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 6-30 (a) and Figure 6-30 (b) shows the phase A source current (Channel 3) and the phase A supply voltage (Channel 4) before and after compensation respectively. The compensated source current is labelled Channel 2. From this it can be seen that reactive power compensation is achieved.

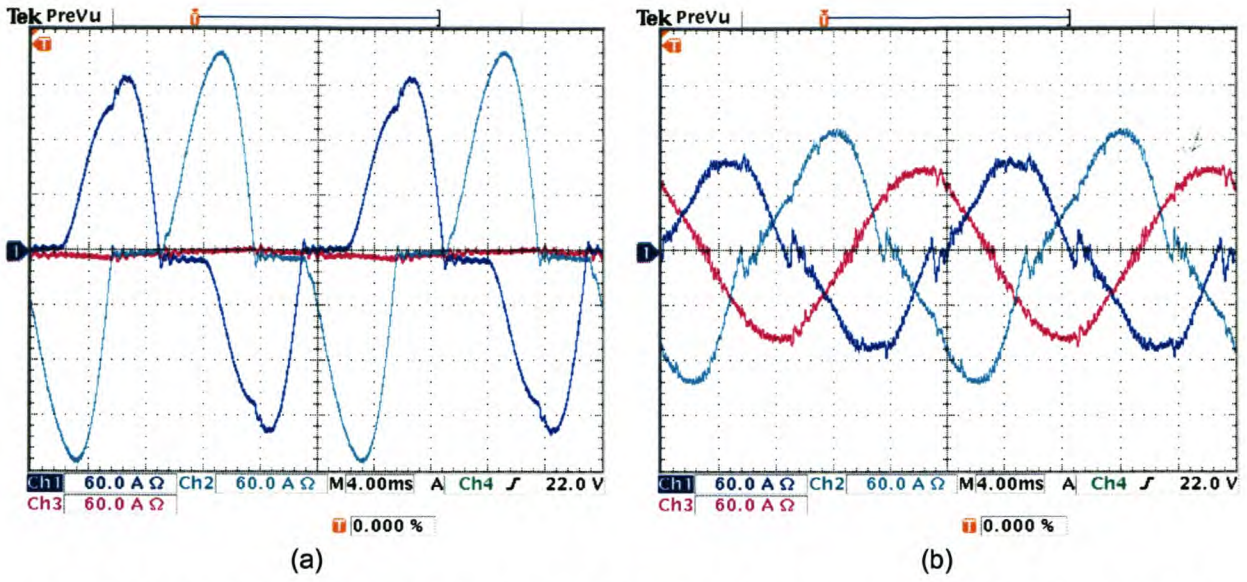


(a) (b)

Figure 6-30 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current

6.4.2 Predictive current controller – with neutral inductor

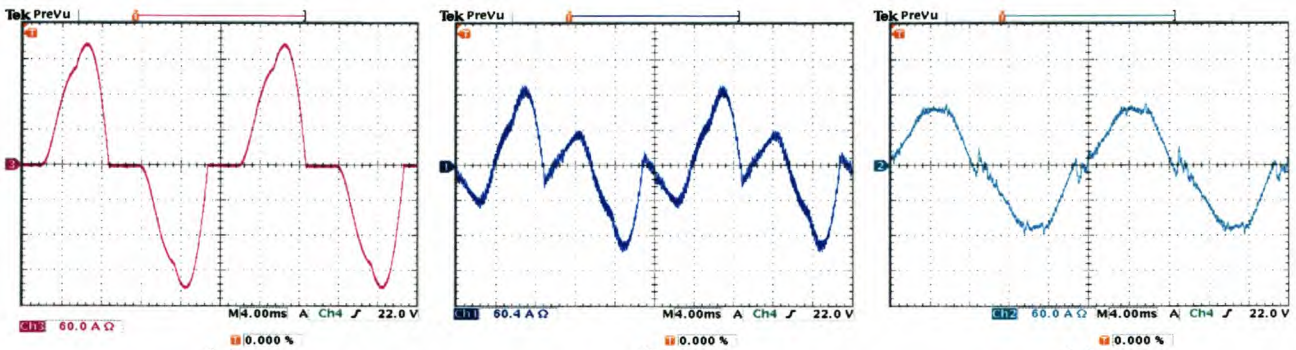
Figure 6-31 (a) and Figure 6-31 (b) illustrate the phase A (Channel 1), B (Channel 2), and C (Channel 3) load currents and the phase A, B and C source currents after compensation respectively. The load currents produce a negative sequence unbalance of 53.2% and a zero sequence unbalance of 48.0%. After compensation the negative sequence unbalance is reduced to 12.0%, and the zero sequence unbalance is reduced to 8.0%. The phase A and B source currents before compensation have a TDD of 35.4% and 43.6% respectively, and after compensation the TDD for phase A is reduced to 9.9%, phase B to 13.3% and phase C to 2.3%.



(a) (b)

Figure 6-31 Practical results showing (a) load current, and (b) compensated source currents

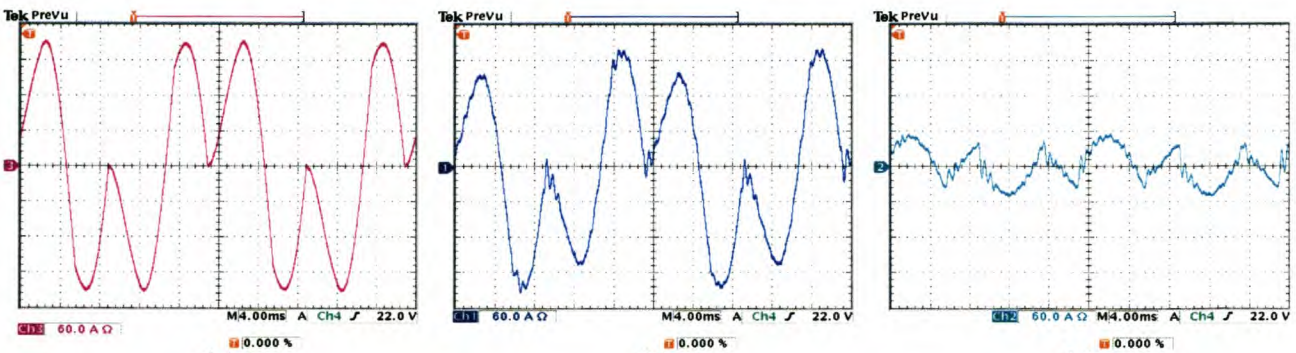
Figure 6-32 (a) shows the load current, and Figure 6-32 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 6-32 (c).



(a) (b) (c)

Figure 6-32 Practical results showing phase A (a) Load current, (b) compensating current, and (c) compensated source current

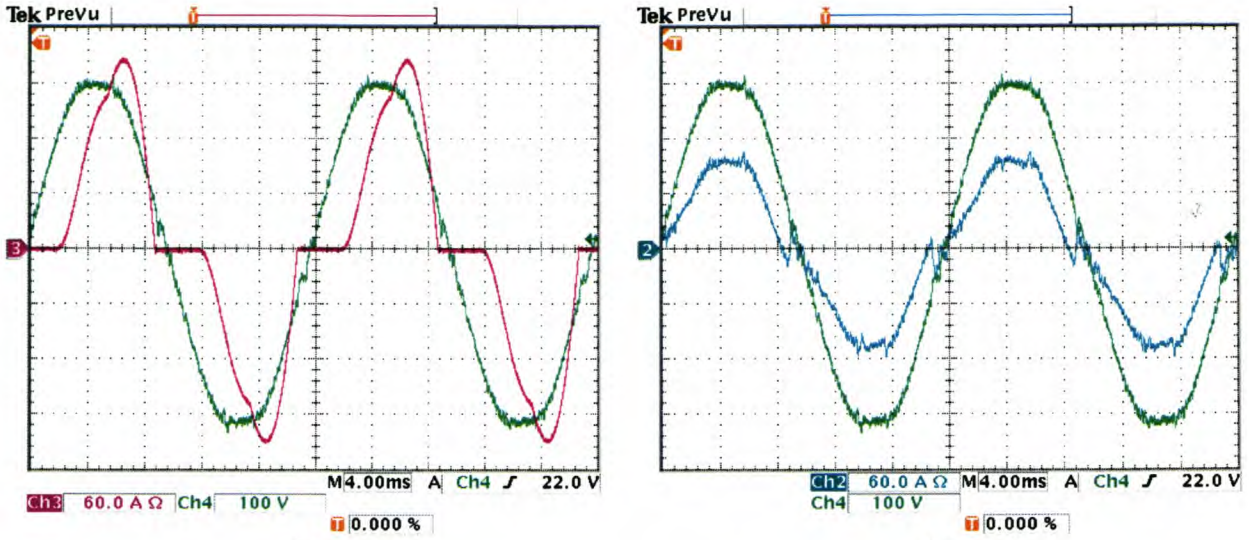
Figure 6-33 (a) shows the uncompensated neutral current, and Figure 6-33 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 6-33 (c).



(a) (b) (c)

Figure 6-33 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 6-34 (a) and Figure 6-34 (b) shows the phase A source current (Channel 3) and the phase A supply voltage (Channel 4) before and after compensation respectively. The compensated source current is labelled Channel 2. From this it can be seen that reactive power compensation is achieved.

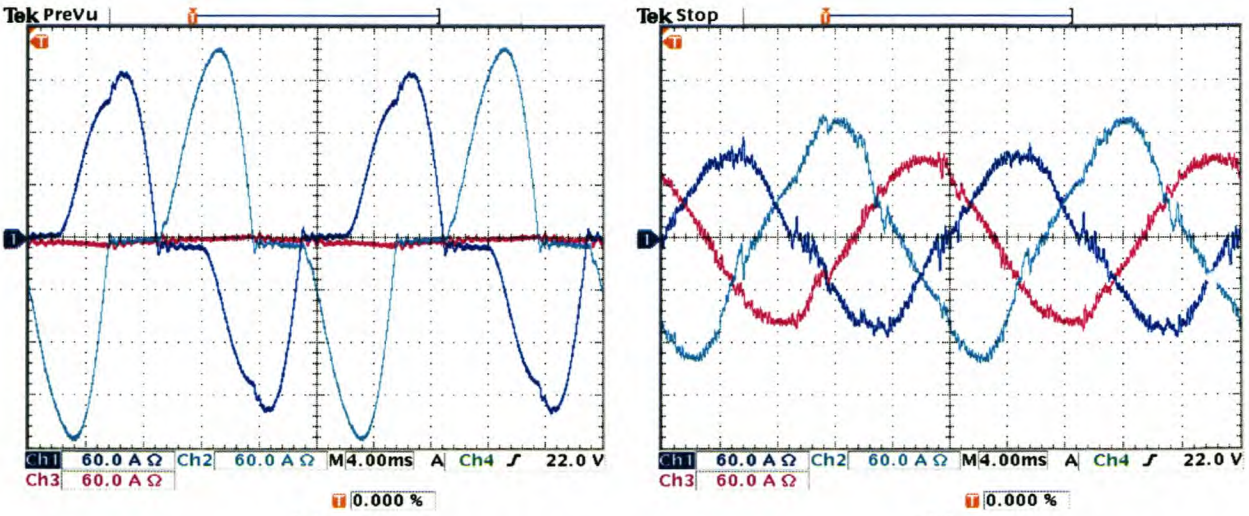


(a) (b)

Figure 6-34 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current

6.4.3 Ideal saturating current controller – without neutral inductor

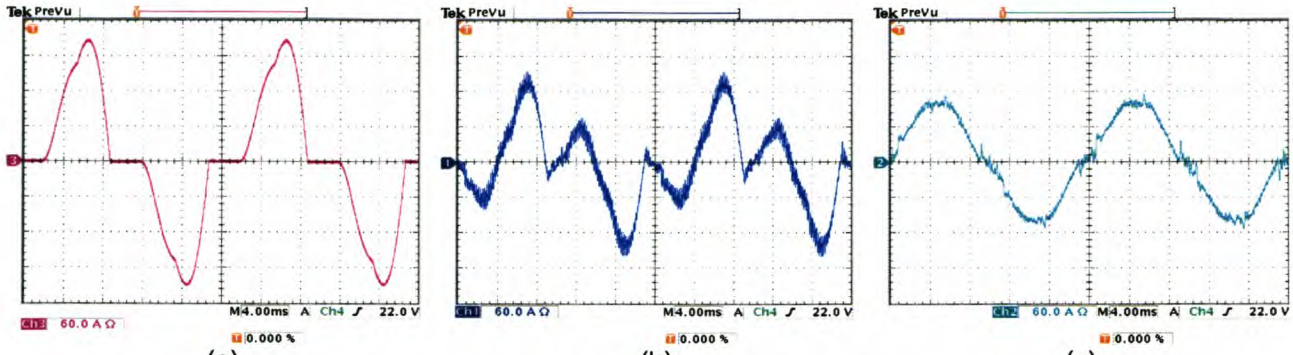
Figure 6-35 (a) and Figure 6-35 (b) illustrate the phase A (Channel 1), B (Channel 2), and C (Channel 3) load currents and the phase A, B and C source currents after compensation respectively. The load currents produce a negative sequence unbalance of 53.2% and a zero sequence unbalance of 48.0%. After compensation the negative sequence unbalance is reduced to 11.1%, and the zero sequence unbalance is reduced to 9.9%. The phase A and B source currents before compensation have a TDD of 35.4% and 43.6% respectively, and after compensation the TDD for phase A is reduced to 7.0%, phase B to 11.6% and phase C to 3.9%.



(a) (b)

Figure 6-35 Practical results showing (a) load current, and (b) compensated source currents

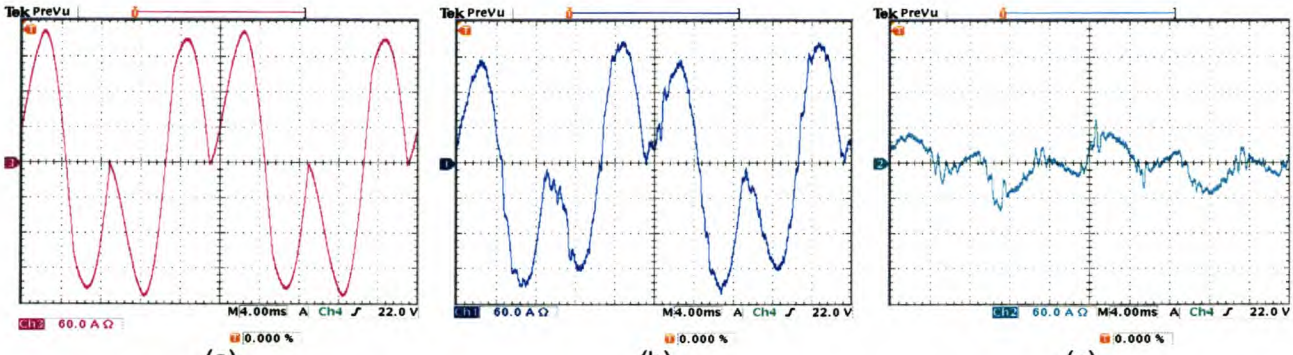
Figure 6-36 (a) shows the load current, and Figure 6-36 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 6-36 (c).



(a) (b) (c)

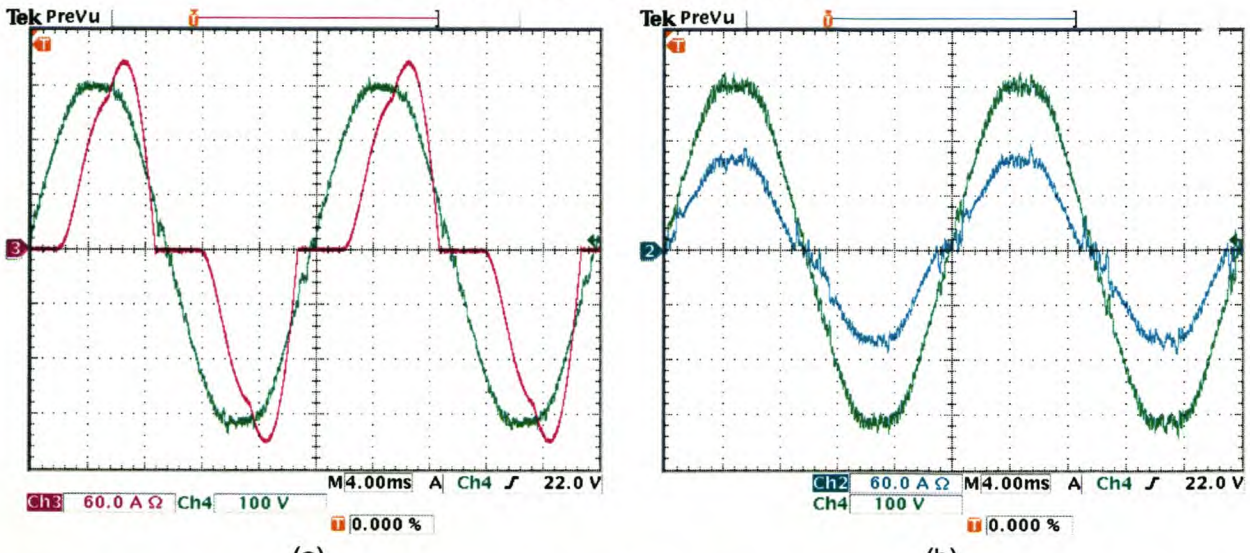
Figure 6-36 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

Figure 6-37 (a) shows the uncompensated neutral current, and Figure 6-37 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 6-37 (c).



(a) (b) (c)

Figure 6-37 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current



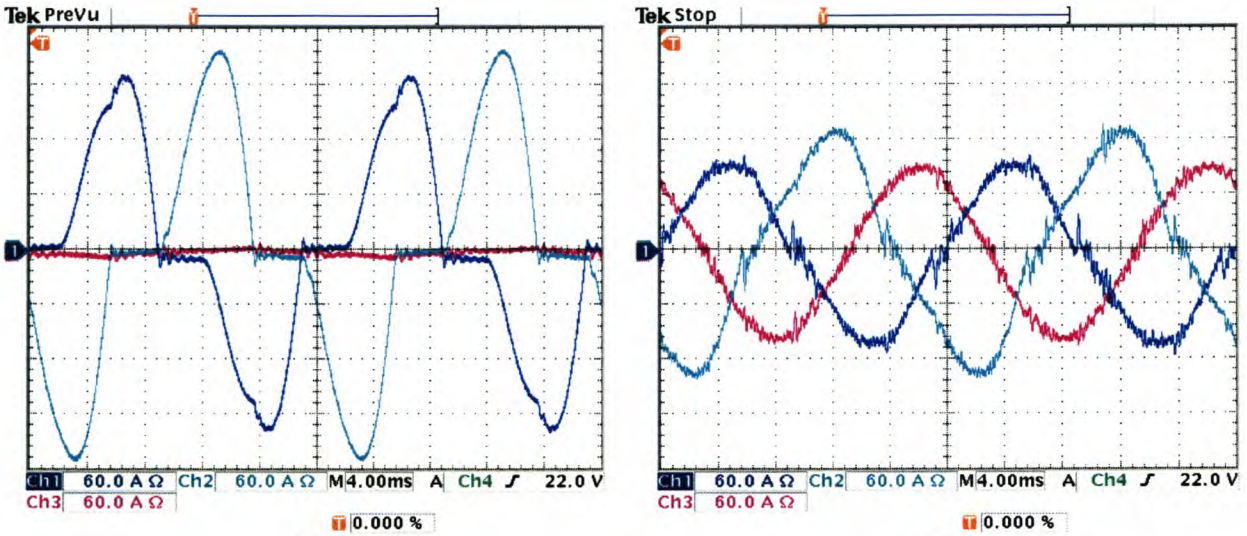
(a) (b)

Figure 6-38 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current

Figure 6-38(a) and Figure 6-38 (b) shows the phase A source current (Channel 3) and the phase A supply voltage (Channel 4) before and after compensation respectively. The compensated source current is labelled Channel 2. From this it can be seen that reactive power compensation is achieved.

6.4.4 Ideal saturating current controller – with neutral inductor

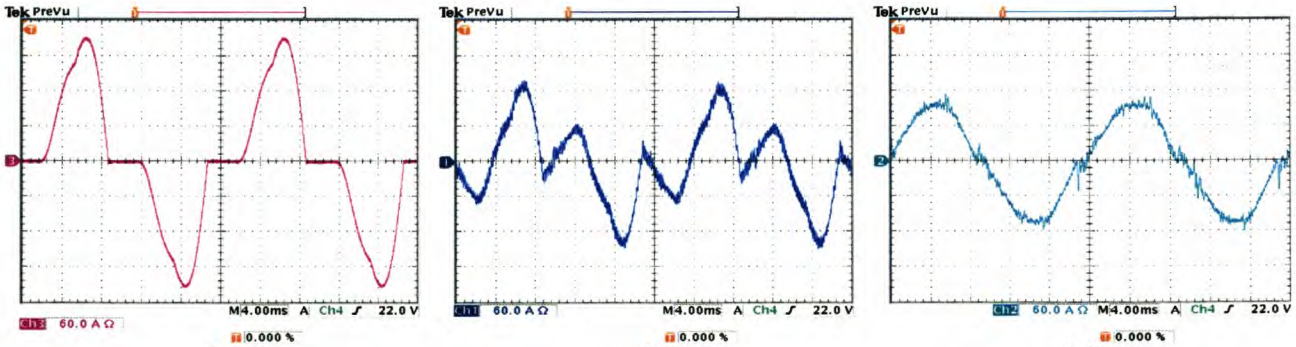
Figure 6-39 (a) and Figure 6-39 (b) illustrate the phase A (Channel 1), B (Channel 2), and C (Channel 3) load currents and the phase A, B and C source currents after compensation respectively. The load currents produce a negative sequence unbalance of 53.2% and a zero sequence unbalance of 48.0%. After compensation the negative sequence unbalance is reduced to 10.6%, and the zero sequence unbalance is reduced to 9.1%. The phase A and B source currents before compensation have a TDD of 35.4% and 43.6% respectively, and after compensation the TDD for phase A is reduced to 6.3%, phase B to 10.6% and phase C to 2.5%.



(a) (b)

Figure 6-39 Practical results showing (a) load current, and (b) compensated source currents

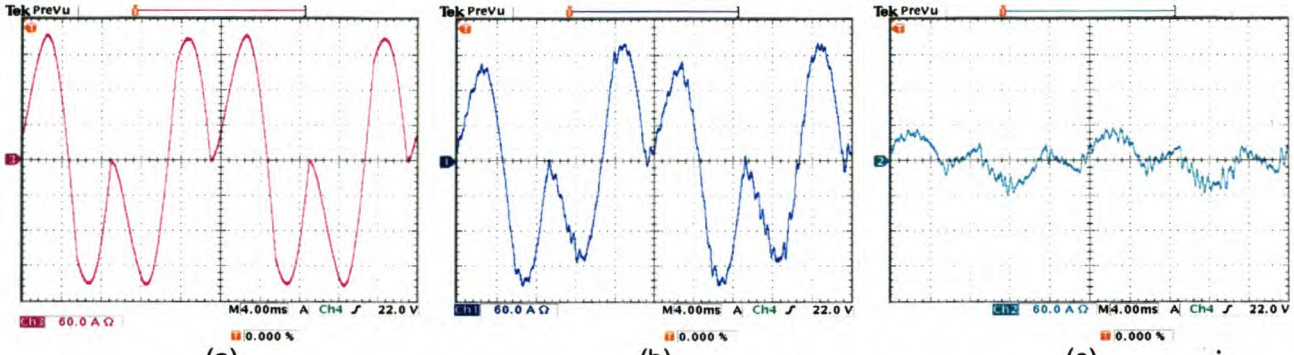
Figure 6-40 (a) shows the load current, and Figure 6-40 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 6-40 (c).



(a) (b) (c)

Figure 6-40 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

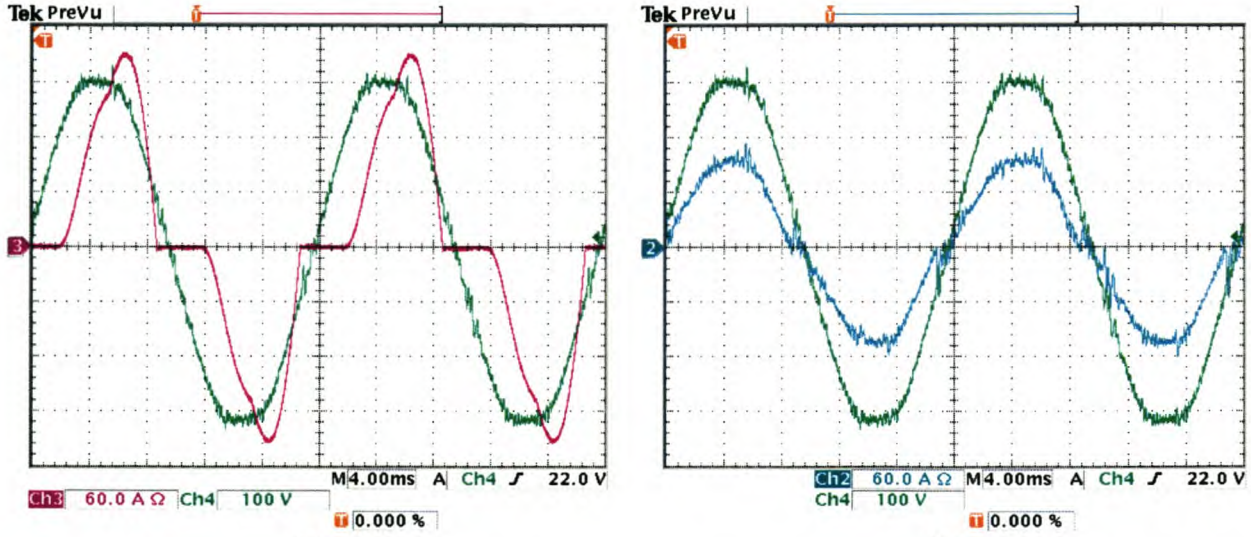
Figure 6-41 (a) shows the uncompensated neutral current, and Figure 6-41 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 6-41 (c).



(a) (b) (c)

Figure 6-41 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 6-42 (a) and Figure 6-42 (b) shows the phase A source current (Channel 3) and the phase A supply voltage (Channel 4) before and after compensation respectively. The compensated source current is labelled Channel 2. From this it can be seen that reactive power compensation is achieved.

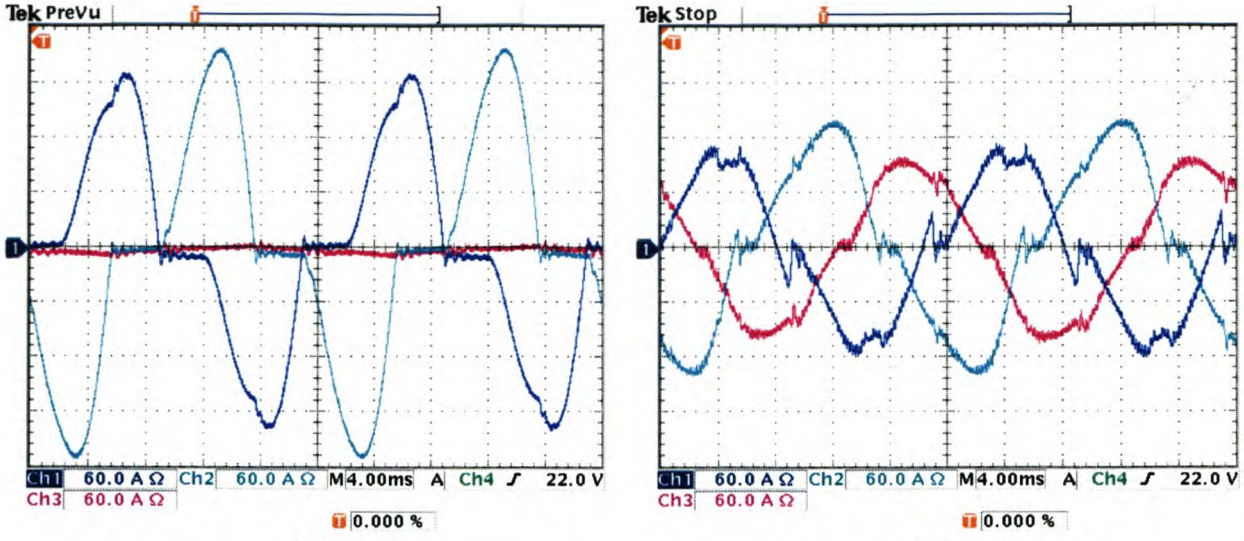


(a) (b)

Figure 6-42 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current

6.4.5 Constant rate current controller – without neutral inductor

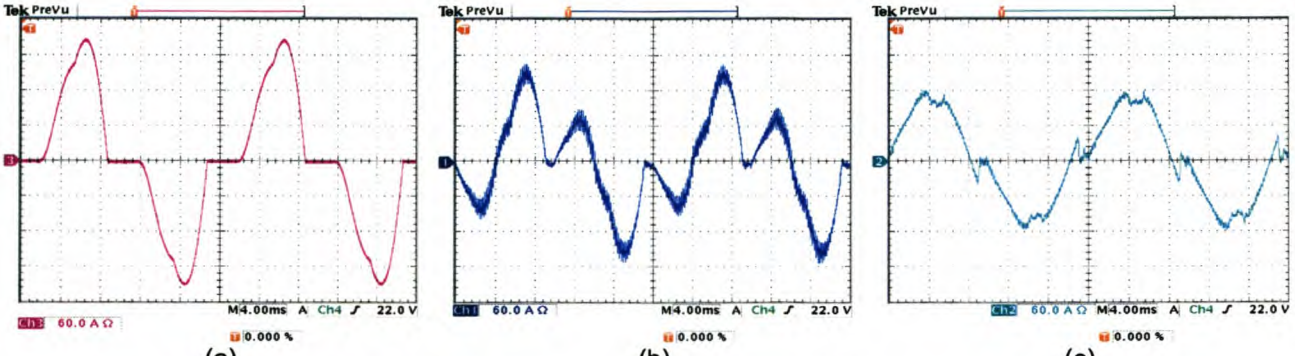
Figure 6-43 (a) and Figure 6-43 (b) illustrate the phase A (Channel 1), B (Channel 2), and C (Channel 3) load currents and the phase A, B and C source currents after compensation respectively. The load currents produce a negative sequence unbalance of 53.2% and a zero sequence unbalance of 48.0%. After compensation the negative sequence unbalance is reduced to 12.3%, and the zero sequence unbalance is reduced to 8.4%. The phase A and B source currents before compensation have a TDD of 35.4% and 43.6% respectively, and after compensation the TDD for phase A is reduced to 13.2%, phase B to 14.6% and phase C to 5.9%.



(a) (b)

Figure 6-43 Practical results showing (a) load current, and (b) compensated source currents

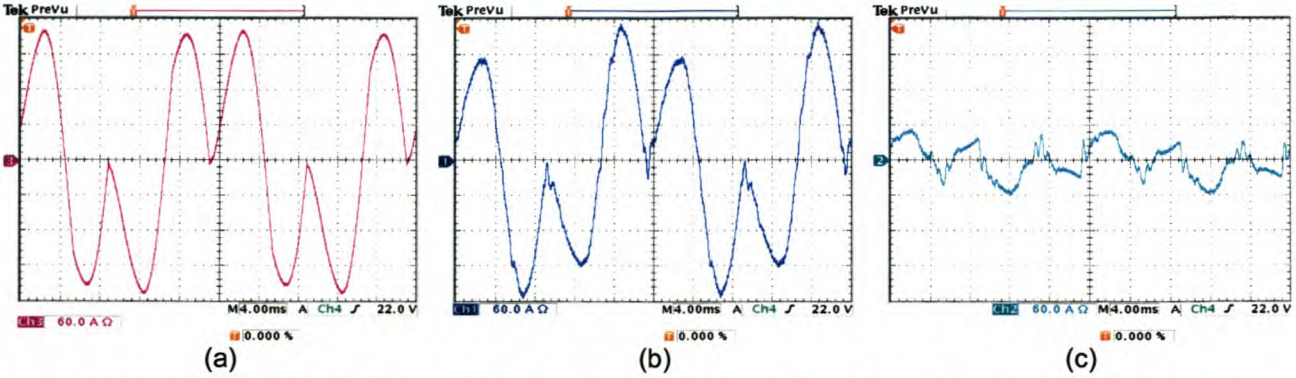
Figure 6-44 (a) shows the load current, and Figure 6-44 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 6-44 (c).



(a) (b) (c)

Figure 6-44 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

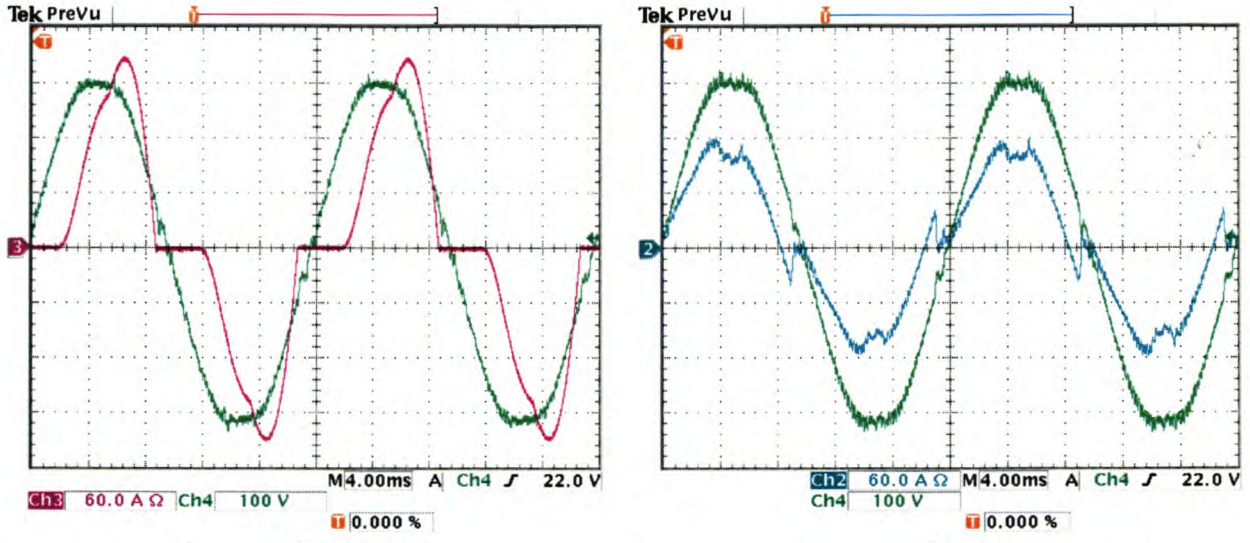
Figure 6-45 (a) shows the uncompensated neutral current, and Figure 6-45 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 6-45 (c).



(a) (b) (c)

Figure 6-45 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 6-46 (a) and Figure 6-46 (b) shows the phase A source current (Channel 3) and the phase A supply voltage (Channel 4) before and after compensation respectively. The compensated source current is labelled Channel 2. From this it can be seen that reactive power compensation is achieved.

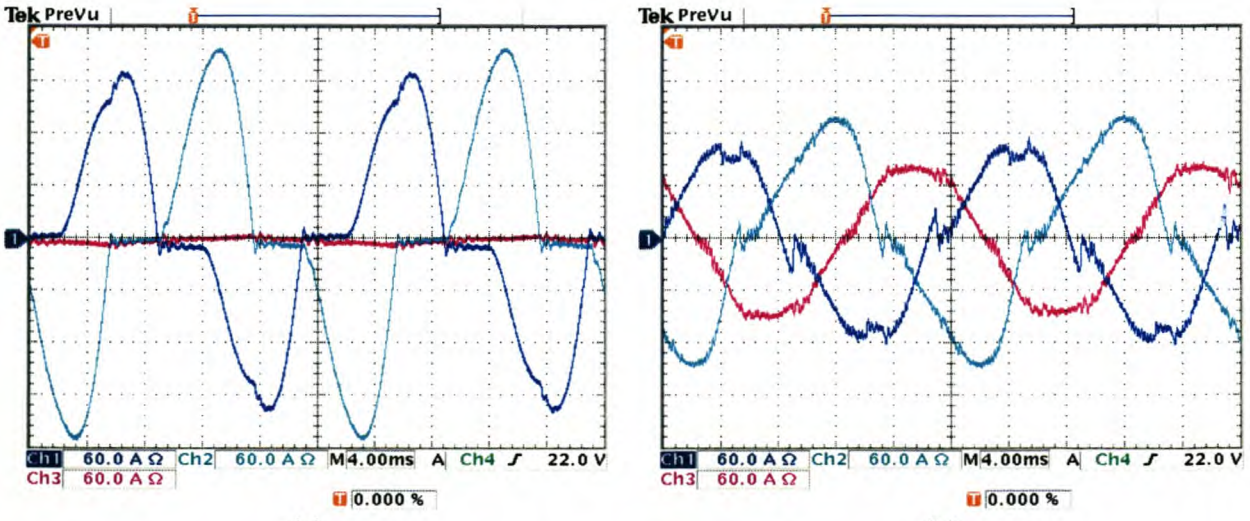


(a) (b)

Figure 6-46 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current

6.4.6 Constant rate current controller – with neutral inductor

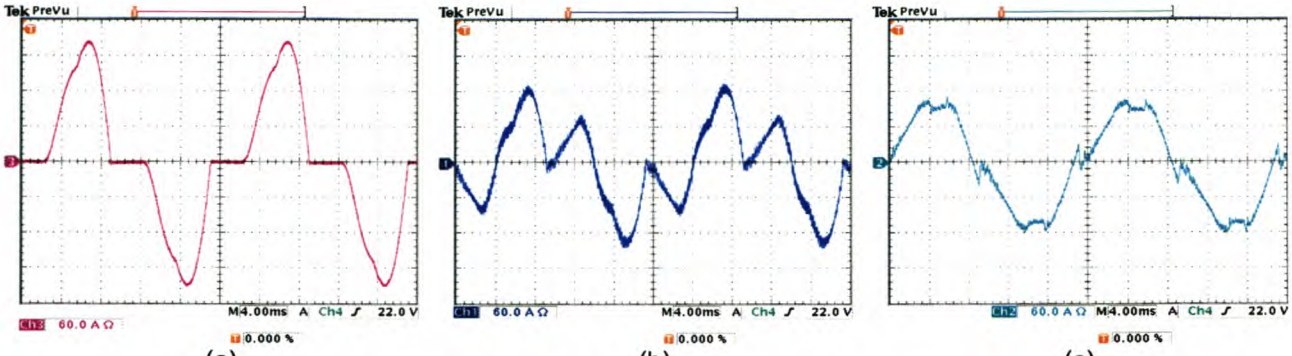
Figure 6-47 (a) and Figure 6-47 (b) illustrate the phase A (Channel 1), B (Channel 2), and C (Channel 3) load currents and the phase A, B and C source currents after compensation respectively. The load currents produce a negative sequence unbalance of 53.2% and a zero sequence unbalance of 48.0%. After compensation the negative sequence unbalance is reduced to 13.8%, and the zero sequence unbalance is reduced to 8.7%. The phase A and B source currents before compensation have a TDD of 35.4% and 43.6% respectively, and after compensation the TDD for phase A is reduced to 11.4%, phase B to 15.6% and phase C to 3.7%.



(a) (b)

Figure 6-47 Practical results showing (a) load current, and (b) compensated source currents

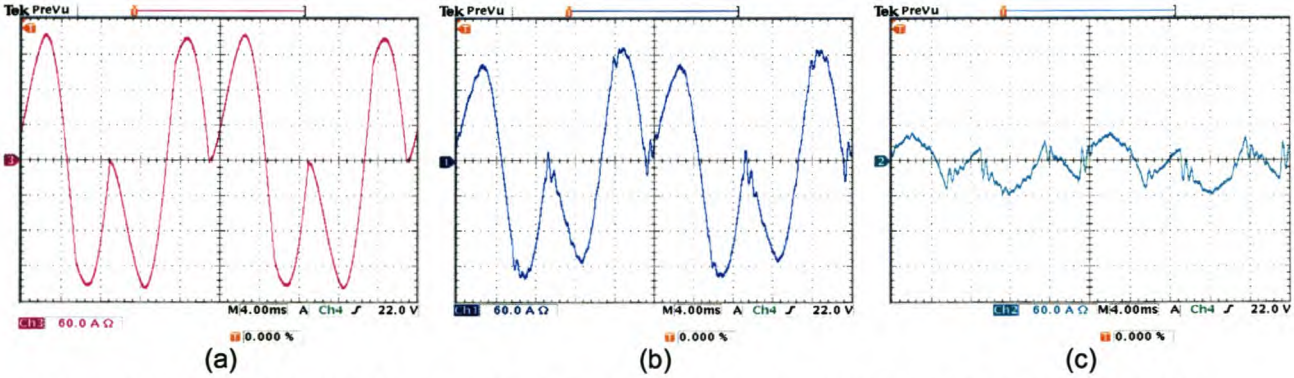
Figure 6-48 (a) shows the load current, and Figure 6-48 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 6-48 (c).



(a) (b) (c)

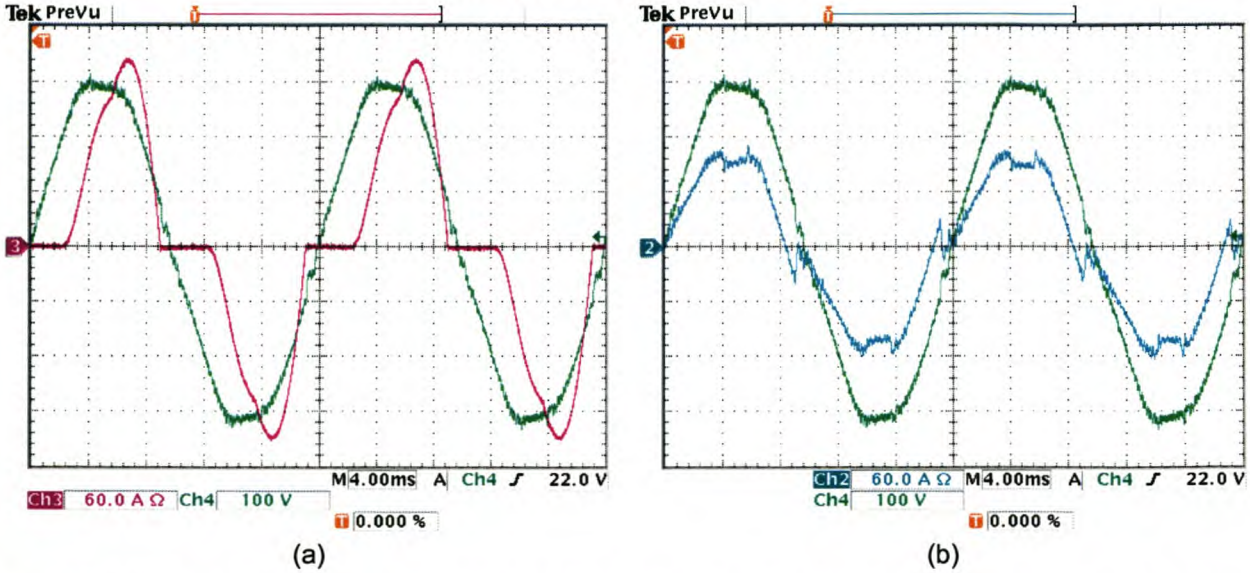
Figure 6-48 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

Figure 6-49 (a) shows the uncompensated neutral current, and Figure 6-49 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 6-49 (c).



(a) (b) (c)

Figure 6-49 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current



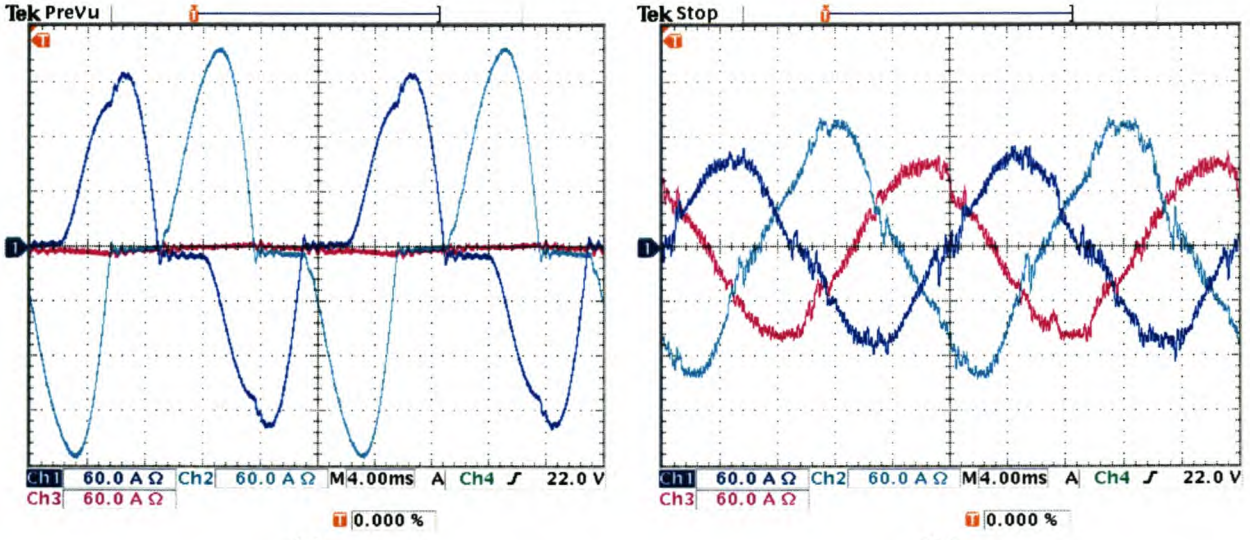
(a) (b)

Figure 6-50 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current

Figure 6-50 (a) and Figure 6-50 (b) shows the phase A source current (Channel 3) and the phase A supply voltage (Channel 4) before and after compensation respectively. The compensated source current is labelled Channel 2. From this it can be seen that reactive power compensation is achieved.

6.4.7 Constant rate plus proportional current controller – without neutral inductor

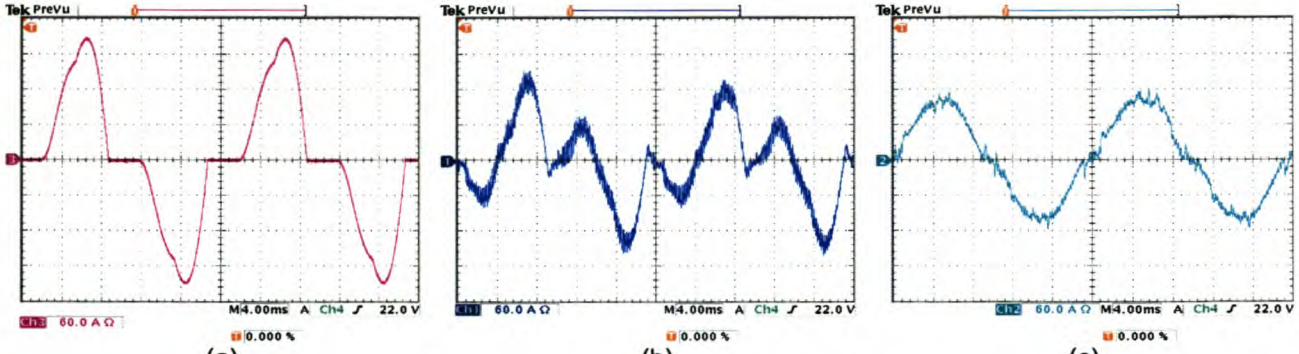
Figure 6-51 (a) and Figure 6-51 (b) illustrate the phase A (Channel 1), B (Channel 2), and C (Channel 3) load currents and the phase A, B and C source currents after compensation respectively. The load currents produce a negative sequence unbalance of 53.2% and a zero sequence unbalance of 48.0%. After compensation the negative sequence unbalance is reduced to 11.1%, and the zero sequence unbalance is reduced to 9.7%. The phase A and B source currents before compensation have a TDD of 35.4% and 43.6% respectively, and after compensation the TDD for phase A is reduced to 7.3%, phase B to 11.6% and phase C to 4.8%.



(a) (b)

Figure 6-51 Practical results showing (a) load current, and (b) compensated source currents

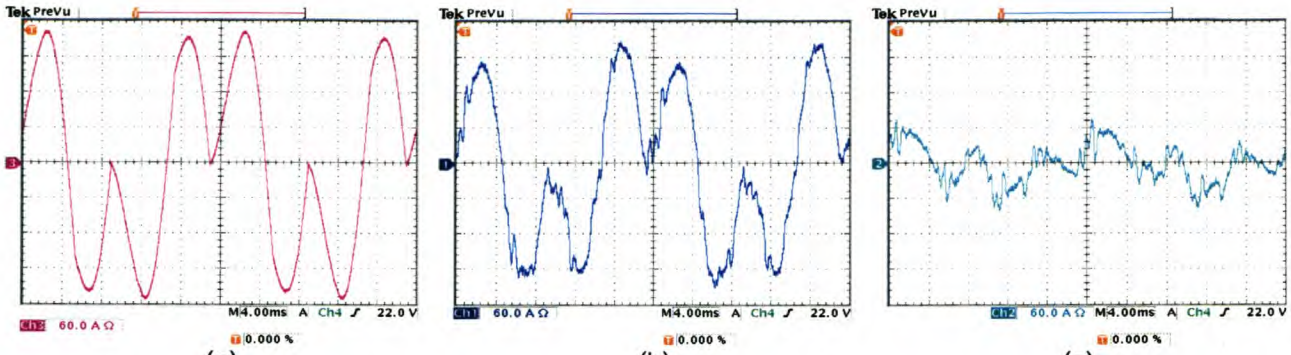
Figure 6-52 (a) shows the load current, and Figure 6-52 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 6-52(c).



(a) (b) (c)

Figure 6-52 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

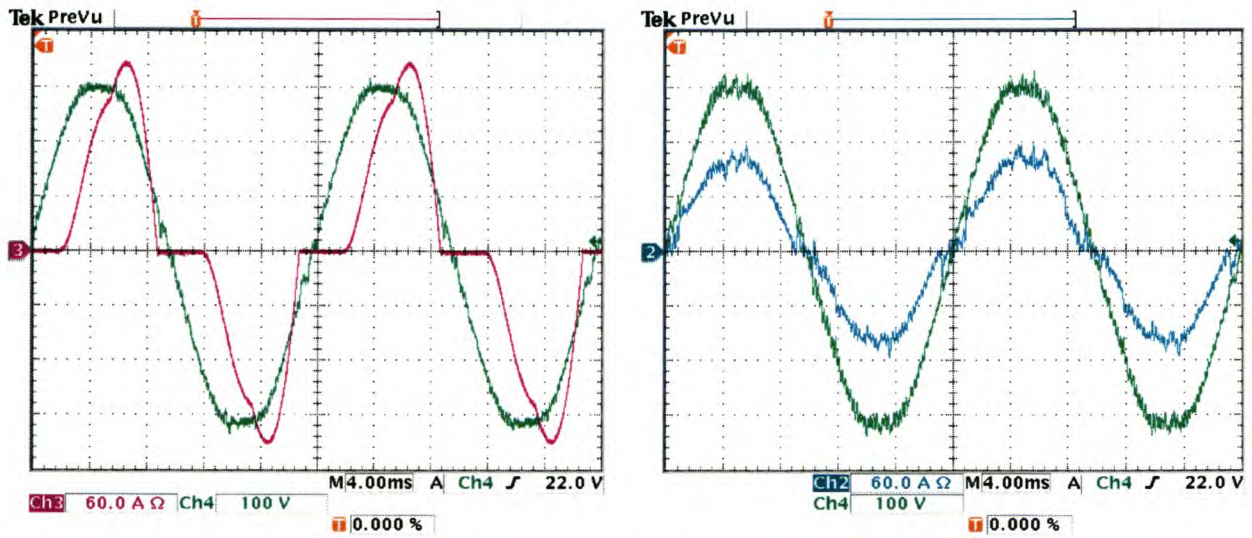
Figure 6-53 (a) shows the uncompensated neutral current, and Figure 6-53 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 6-53 (c).



(a) (b) (c)

Figure 6-53 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 6-54 (a) and Figure 6-54 (b) shows the phase A source current (Channel 3) and the phase A supply voltage (Channel 4) before and after compensation respectively. The compensated source current is labelled Channel 2. From this it can be seen that reactive power compensation is achieved.

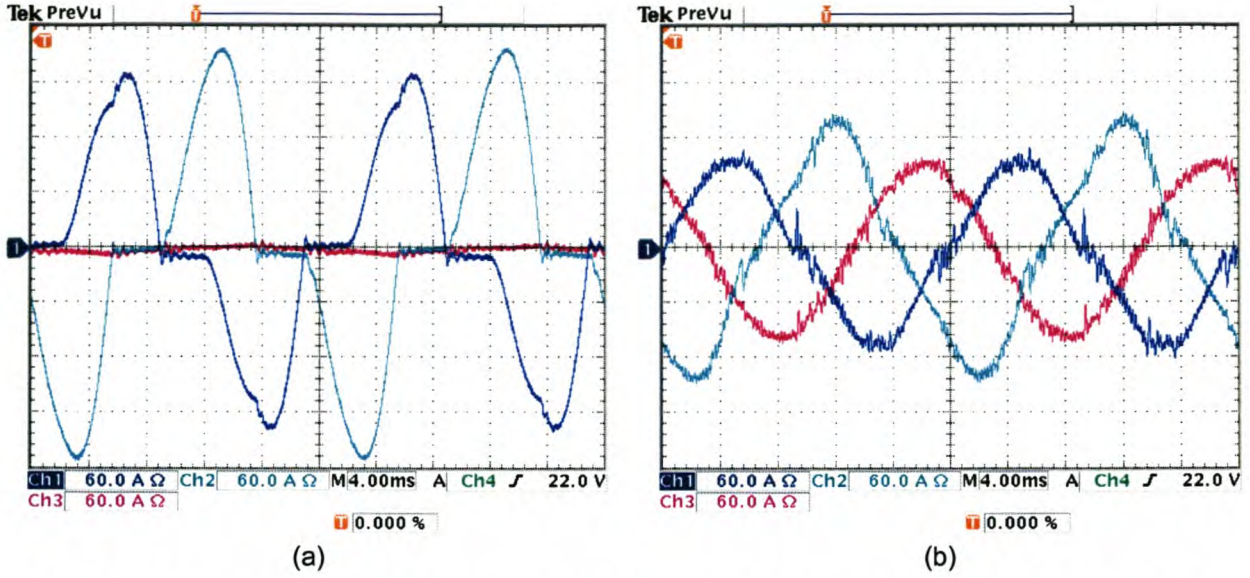


(a) (b)

Figure 6-54 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current

6.4.8 Constant rate plus proportional current controller – with neutral inductor

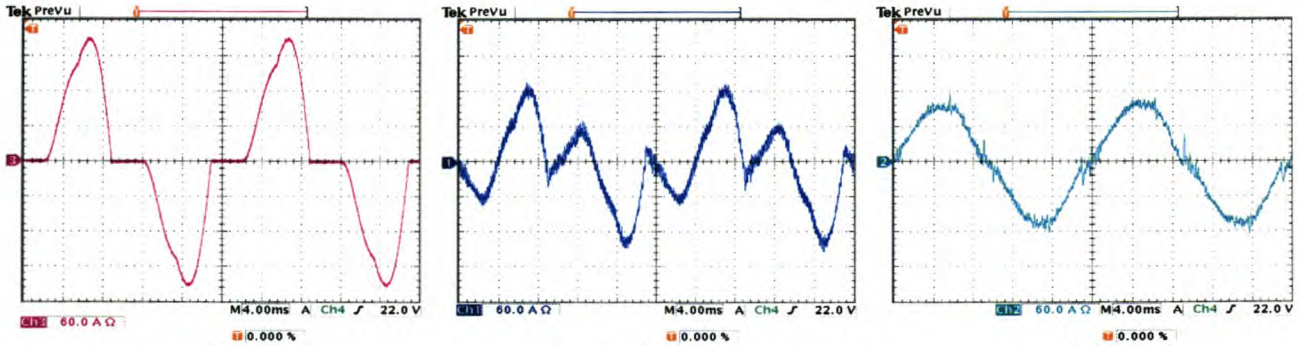
Figure 6-55 (a) and Figure 6-55 (b) illustrate the phase A (Channel 1), B (Channel 2), and C (Channel 3) load currents and the phase A, B and C source currents after compensation respectively. The load currents produce a negative sequence unbalance of 53.2% and a zero sequence unbalance of 48.0%. After compensation the negative sequence unbalance is reduced to 10.9%, and the zero sequence unbalance is reduced to 9.8%. The phase A and B source currents before compensation have a TDD of 35.4% and 43.6% respectively, and after compensation the TDD for phase A is reduced to 6.9%, phase B to 11.6% and phase C to 2.7%.



(a) (b)

Figure 6-55 Practical results showing (a) load current, and (b) compensated source currents

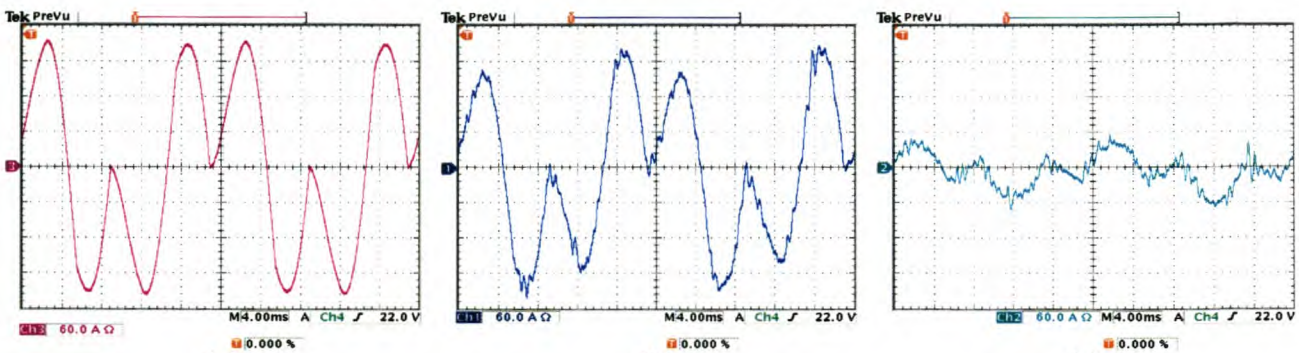
Figure 6-56 (a) shows the load current, and Figure 6-56 (b) shows the current that is injected by the inverter to realise the compensated phase A source current shown in Figure 6-56 (c).



(a) (b) (c)

Figure 6-56 Practical results showing phase A (a) load current, (b) compensating current, and (c) compensated source current

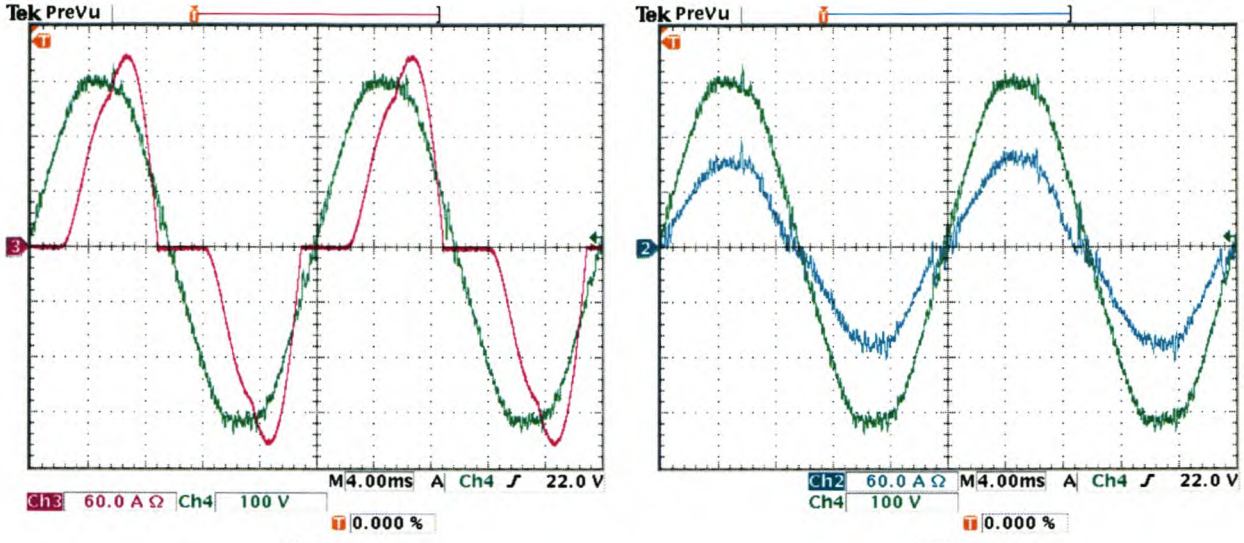
Figure 6-57 (a) shows the uncompensated neutral current, and Figure 6-57 (b) shows the current that is injected by the inverter to realise the compensated neutral current shown in Figure 6-57 (c).



(a) (b) (c)

Figure 6-57 Practical results showing neutral (a) uncompensated current, (b) compensating current, and (c) compensated current

Figure 6-58 (a) and Figure 6-58 (b) shows the phase A source current (Channel 3) and the phase A supply voltage (Channel 4) before and after compensation respectively. The compensated source current is labelled Channel 2. From this it can be seen that reactive power compensation is achieved.



(a) (b)

Figure 6-58 Practical results showing (a) phase A voltage and load current, (b) phase A voltage and compensated source current

6.5 Summary

In this chapter the discussed theory was verified practically.

The three-dimensional space vector PWM modulation technique was found superior in performance to the currently implemented space vector PWM modulating technique regarding realising unbalanced voltages.

The current controllers were implemented practically and the rms current error values found from the difference between the reference current components and the actual current components are summarised in Table 20. The rms current error values are lower in the practical system when compared to the simulations shown in Table 17. This can be attributed to the non-idealities that are not taken into consideration in the simulation model, and that cause damping effects in the practical system. Overall the results compare favorable to the simulation results shown in Chapter 5, thus the working of the current controllers are verified.

Table 20 – Summary of the rms current error values

Type of control	Phase A		Phase B		Phase C	
	Sinusoidal	Square	Sinusoidal	Square	Sinusoidal	Square
Predictive current control without any compensation (Without neutral inductor)	4.5	17.2	3.4	11.5	1.9	8.6
Predictive current control without any compensation (With neutral inductor)	4.3	15.0	3.4	11.4	2.5	11.0
Predictive current control with time delay compensation (Without neutral inductor)	12.4	13.6	7.6	10.8	2.8	9.2
Predictive current control with time delay compensation (With neutral inductor)	8.7	10.5	6.6	9.6	4.7	7.7
Predictive current control with time delay and dead-time compensation (Without neutral inductor)	1.7	7.4	1.7	7.5	1.2	4.7
Predictive current control with time delay and dead-time compensation (With neutral inductor)	1.6	8.1	1.5	7.5	1.0	4.6
Ideal saturating control with time delay and dead-time compensation (Without neutral inductor)	0.6	7.6	0.9	8.0	0.9	6.2
Ideal saturating control with time delay and dead-time compensation (With neutral inductor)	0.5	8.4	0.8	7.8	0.7	4.7
Constant rate control with time delay and dead-time compensation (Without neutral inductor)	0.8	7.4	1.2	7.7	1.1	4.9
Constant rate control with time delay and dead-time compensation (With neutral inductor)	0.6	11.9	0.9	7.6	0.8	5.3
Constant rate plus proportional control with time delay and dead-time compensation (Without neutral inductor)	0.6	8.0	1.0	8.5	0.8	6.8
Constant rate plus proportional control with time delay and dead-time compensation (With neutral inductor)	0.8	8.2	0.9	7.7	0.7	4.7

When the current controllers are implemented into the shunt active power filter the results does not compare that favorable to the simulation results. The TDD values and the unbalance values shown in Table 21 and Table 22 respectively, are a lot higher than in the simulation results. This can be attributed to noise effects that is not taken into consideration in the simulation model, and the assumption that is made that the EMF voltage is constant during a switching period, when it is in fact varying quite considerably. The noise effects is quite a big problem especially when the neutral inductor is not connected.

Table 21 – Summary of the TDD values for the different current controllers

Type of control	Phase A [%]	Phase B [%]	Phase C [%]
Predictive current control with time delay and dead-time compensation (Without neutral inductor)	10.3	14.0	3.1
Predictive current control with time delay and dead-time compensation (With neutral inductor)	9.9	13.3	2.3
Ideal saturating control with time delay and dead-time compensation (Without neutral inductor)	7.0	11.6	3.9
Ideal saturating control with time delay and dead-time compensation (With neutral inductor)	6.3	10.6	2.5
Constant rate control with time delay and dead-time compensation (Without neutral inductor)	13.2	14.6	5.9
Constant rate control with time delay and dead-time compensation (With neutral inductor)	11.4	15.6	3.7
Constant rate plus proportional control with time delay and dead-time compensation (Without neutral inductor)	7.3	11.6	4.8
Constant rate plus proportional control with time delay and dead-time compensation (With neutral inductor)	6.9	11.6	2.7

Table 22 – Summary of the unbalance values for the different current controllers

Type of control	Negative sequence unbalance [%]	Zero sequence unbalance [%]
Predictive current control with time delay and dead-time compensation (Without neutral inductor)	12.1	7.6
Predictive current control with time delay and dead-time compensation (With neutral inductor)	12.0	8.0
Ideal saturating control with time delay and dead-time compensation (Without neutral inductor)	11.1	9.9
Ideal saturating control with time delay and dead-time compensation (With neutral inductor)	10.6	9.1
Constant rate control with time delay and dead-time compensation (Without neutral inductor)	12.3	8.4
Constant rate control with time delay and dead-time compensation (With neutral inductor)	13.8	8.7
Constant rate plus proportional control with time delay and dead-time compensation (Without neutral inductor)	11.1	9.7
Constant rate plus proportional control with time delay and dead-time compensation (With neutral inductor)	10.9	9.8

When the TDD distortion values shown in Table 21 is considered it can be seen that the current controllers which have the best performance are respectively the ideal saturating current controller and the constant rate plus proportional current controller with the neutral inductor connected.

7. Conclusions and recommendations

7.1 Power-circuit configuration selection and modelling

Various power circuit configurations were discussed, which are utilised in active harmonic compensation. A three-phase four-wire topology was developed in the dqo space, and a true three-dimensional space vector PWM voltage control scheme was developed in order to adequately address the problem of switching a three-phase four-leg inverter.

The dynamic system model in the stationary dq0 space for the three-phase four-wire topology as proposed by [12] was proven incorrect, and the correct dynamic model was developed, which also takes the effect of the neutral inductor into consideration.

7.2 Reference signal generating algorithms

Two reference signal-generating algorithms were discussed, namely the generalised instantaneous reactive power theory and the synchronous reference frame technique.

The synchronous reference frame technique proposed by [25] was expanded to enable the isolation of the zero sequence current component into its instantaneous active and reactive current components.

A time delay compensation method was proposed that will enable the proper prediction of the reference currents in a three-phase four-wire system, and the two discussed reference signal-generating algorithms were analysed under non-ideal conditions. From the simulations results it was concluded that when the supply voltages is unbalanced or distorted, the synchronous reference frame technique offer better results than the generalised reactive power theory.

7.3 Detailed design process for the current controllers

Two categories of reference signal tracking algorithms were investigated, namely predictive current controllers and sliding mode current controllers. The sliding mode current controllers that were considered are the ideal saturating current controller, the constant rate current controller, and the constant rate plus proportional current controller. The detailed design process for these current controllers was provided, and simulation results illustrated that the proposed current controllers work satisfactorily under ideal conditions.

7.4 Practical implications

The practical implementation of the discussed current controllers introduces factors that contribute to the deterioration of the voltage source inverter's ability to achieve proper reference current tracking.

A proper compensating technique was proposed to compensate for the effect that sampling and computational time delay have on the performance of the system. Additionally, an investigation was done into the effect that dead-time has on the performance of the system, and based on this discussion a dead-time compensating strategy was proposed, which enables the proper compensation for dead-time in

a three-phase four-wire voltage source inverter, even when a current changes direction during a switching cycle.

A detailed analysis was also done through simulation on the proposed current controllers taking practical issues into consideration. Two sets of current references were applied to test the performance of the current controllers. Sinusoidal references were applied to test the tracking performance of the controller when the rate of current change is relatively small, and square waveforms were applied to investigate the performance of the controller when the rate of current change is high (step response).

Finally the shunt active power filter performance was investigated through simulation by applying the discussed theories.

7.5 Practical results of theory presented

Practical results were provided to confirm the discussed theories. The new proposed three-dimensional space vector PWM technique was found to be superior in performance to the currently implemented space vector PWM technique when unbalanced reference currents needs to be tracked. The proposed current controller's performance through simulations was validated by the practical results.

Table 23 – Summary of the TDD values for the different current controllers

Type of control	Phase A [%]	Phase B [%]	Phase C [%]
Uncompensated load current	35.4	43.6	0
Predictive current control with time delay and dead-time compensation (Without neutral inductor)	10.3	14.0	3.1
Predictive current control with time delay and dead-time compensation (With neutral inductor)	9.9	13.3	2.3
Ideal saturating control with time delay and dead-time compensation (Without neutral inductor)	7.0	11.6	3.9
Ideal saturating control with time delay and dead-time compensation (With neutral inductor)	6.3	10.6	2.5
Constant rate control with time delay and dead-time compensation (Without neutral inductor)	13.2	14.6	5.9
Constant rate control with time delay and dead-time compensation (With neutral inductor)	11.4	15.6	3.7
Constant rate plus proportional control with time delay and dead-time compensation (Without neutral inductor)	7.3	11.6	4.8
Constant rate plus proportional control with time delay and dead-time compensation (With neutral inductor)	6.9	11.6	2.7

Lastly, the shunt active power filters were implemented practically and their operation confirmed. It was found that the simulation and practical results differ when the current controllers were implemented in a shunt active power filter. This is due to the noise effects and the EMF voltage that is assumed constant during a switching period when it is in fact varying considerably. A summary of the TDD values for the different current controllers is shown in Table 23. It was found that the best current controllers for a shunt active power filter in this application are the ideal saturating sliding mode current controller and the constant rate plus proportional sliding mode current controller. It must also be noted that better performance was obtained when the neutral inductor was connected.

7.6 Recommendations and future work

When the discussed theory was implemented practically the performance of the current controllers was limited by the controller hardware. The prediction of the reference current signals, as was discussed in Chapter 3, couldn't be implemented practically due to the lack of processing time available from the DSP.

Throughout this thesis the assumption is made that the EMF voltage is considered to be constant during a sample period. This is not always a valid assumption, especially when there is a sudden step change in the load currents. This EMF voltage plays a major role in the performance of current controllers, and in order to compensate for the changing of the EMF voltage during a sample period, the controller must be redesigned to enable over-sampling. Currently the controller boards' A/D converters outputs are connected onto the data bus of the controller; thus over-sampling is impossible unless it interferes with the operation of the DSP. This is not an option in the currently used DSP since the DSP is already running out of processing time as is.

7.7 Summary

This thesis investigated successfully the implementation of shunt active power filtering algorithms for unbalanced, non-linear loads. Four different types of current controllers were developed to achieve active power filtering utilising a three-phase four-leg voltage source inverter. The current controller's performance was investigated by simulation and the theory was validated by implementing it in a practical system.

References

Standards, Journal and Conference Papers

[1] Thomas S. Key, Jih-Sheng Lai "Comparison of Standards and Power Supply Design Options for limiting Harmonic Distortion in Power Systems", *IEEE Transactions on Industry Applications*, Vol 29, No. 4, pp. 688-695, July/August 1993

[2] J. Afonso, C. Couto, J. Martins, "Active filters with control based on the p-q Theory," *IEEE Industrial Electronics Newsletter*, Vol 47, September 2000

[3] B. Singh, K. Al-Haddad, A. Chandra, " A review of active filters for power Quality improvement," *IEEE Transactions on Industry Applications*, Vol 46, No. 5, pp 960-971, October 1999

[4] G. Ledwich, "Current source inverter modulation," *IEEE Transactions on Power Electronics*, Vol 6, No. 4, pp 618-623, October 1991

[5] H. Akagi, "Trends in active power line conditioners," *IEEE Transactions on Power Electronics*, Vol. 9, pp 263-268, May 1994

[6] S.T. Senini, P.J. Wolfs, "Systematic Identification and review of hybrid active filter topologies," *in Proc. IEEE PESC'02, 2002*, pp. 394-399

[7] R. Zhang, "High performance power converter systems for non-linear and unbalanced load/source," *Ph.D Dissertation, Virginia Polytechnic Institute and State University*, 1998

[8] T.S. Key, J-S. Lay, "Comparison of standards and Power Supply Design Options for limiting Harmonic Distortion in Power systems," *IEEE Transactions on Industry Applications*, Vol 29, No. 4, pp 688-695, July/August 1993

[9] NRS 048-1/2/3/4:1996, "Rationalized User Specification," Electricity Supply- Quality of Supply Standards

[10] IEEE Std 519-1992, " IEEE recommended practice and requirements for harmonic control in electrical power systems," IEEE, new York (U.S.A.), 1993

[11] "Guide for applying Harmonic limits on Power systems," Harmonics working group, P159A Task Force, May 1996

[12] M.J. Ryan, "Analysis, modelling and control of three-phase, four-wire sine wave inverter systems," *Ph.D. dissertation, Elect. Comput. Eng. Dep., Univ. Wisconsin, Madison*, 1997

[13] F.Z. Peng, "Harmonic Sources and filtering Approaches," *Transactions on Industry Applications Magazine*, pp 18-25, Jul/Aug 2001

[14] H.W. van der Broeck, H.C. Skudelny, G.V. Stanke, " Analysis and Realization of a pulsewidth modulator based on voltage space vectors," *IEEE Transactions on Industry Applications*, Vol 24, No. 1, pp 142-150, January/February 1988

[15] R.F. de Camargo, F. Botteron, H.L. Hey, H.A. Grundling, J.R. Pinheiro, H. Pinheiro, "New limiting algorithms for space vector modulated three-phase four-leg voltage source inverter", *in Proc. PESC'02,* 2002, Vol.1, pp. 232-237

[16] J.W. Kolar, H. Ertl, F.Z. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM Converter system, ","*IEEE Transactions on Industry Applications*, Vol 27, No. 6, pp 1063-1075, November/December 1991

[17] H. Prasad, "Analysis and comparison of space vector modulation schemes for three-leg and four-leg voltage source inverters, "*M.S. Thesis, Virginia Polytechnic Institute and State University*, 1997

[18] F.Z. Peng, J.S. Lai, "Generalized Instantaneous reactive power theory for three phase power systems, " *IEEE Transactions on Instrumentation and Measurements*, Vol. 45, No. 1, pp 293-297, February 1996

[19] H. Akagi, Y. Kanazawa, A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components, " *IEEE Transactions on Industry Applications*, Vol. 20, No. 3, pp 625-630, May/June 1984

[20] J.L. Willems, "A new interpretation of the Akagi-Nabae power components of nonsinusoidal three-phase situations, " *IEEE Transactions on Instrumentation and Measurements*, Vol. 41, No. 4, pp 523-527, August 1992

[21] F.Z. Peng, G.W. Ott, Jr. and Donald J. Adams, "Harmonic and Reactive Power Compensation Based on the Generalized Instantaneous Reactive Power Theory for Three-Phase Four-Wire systems," *IEEE Transactions on Power Electronics*, Vol. 13, No. 6, pp. 1174-1181, November 1998

[22] Robert Koch. Eskom TSI, Private discussion, 11 September 2003

[23] CENELEC EN 50160, "Voltage characteristics of electricity supplied by public distribution systems, " November 1999

[24] J.J. Uys, "Dynamic digital control schemes for three phase UPS inverters, " *M.Sc. Eng. Thesis, University of Stellenbosch*, November 2002

[25] A. Nabae, T. Tanaka, "A new definition of instantaneous Active-reactive current and power based on instantaneous space vectors on polar coordinates in three-phase circuits, " *IEEE Transactions on Power Delivery*, Vol. 11, No. 3, pp. 1238-1243, July 1996

[26] S. Buso, L. Malesani, P. Mattavelli, "Comparison of current control techniques for active filter applications" *IEEE Transactions on Industrial Electronics*, Vol. 45, No. 5, pp. 722-729, October 1998

[27] S. Buso, S. Fasolo,L. Malesani, P. Mattavelli, "A dead-beat adaptive hysteresis current control, "*IEEE Transactions on Industry Applications*, Vol. 36, No. 4, pp 1174-1180, July/August 2000

[28] M. P. Kazmierkowzi, L. Malesani, "Current control Techniques for three-phase voltage source PWM converters: A survey, "*IEEE Transactions on Industrial Electronics*, vol. 45, no. 5, pp. 691-703, October 1998

[29] T.G. Habetler, "A space vector-based rectifier regulator for AC/DC/AC Converters, " *IEEE Transactions on Power Electronics*, Vol 8, No. 1, pp.30-36, January 1993.

[30] P. Mattavelli, "A closed loop selective harmonic compensation for active filters, "*IEEE Transactions on Industry Applications*, Vol. 37, No. 1, pp 81-89, January/February 2001

[31] J. Svenson, R. Ottersten, "Shunt active filtering of vector current controlled VSC at a moderate switching frequency," *IEEE Transactions on Industry Applications*, Vol. 35, No. 5, pp 1083-1090, September/October 1999

[32] F. Abrahamsen, A. David, "Adjustable Speed drive with active filtering capability for harmonic current compensation, "*in Proc. IEEE PESC'95*, , Vol 2, pp. 1137-1143, June 1995

[33] R.A. Gannett, J.C. Sozio, D. Boroyevich, "Application of synchronous and stationary frame controllers for unbalanced and non-linear load compensation in 4-leg inverters," CPES 2002, pp. 119-124, 2002

[34] B. Bae, S. Sul, "A compensation method for time delay of full-digital synchronous frame current regulator of PWM AC drives," *IEEE Transactions on Industry Applications*, Vol. 39, No. pp 802-810, May/June 2003

[35] W.S. Oh, Y.T. Kim, H.J. Kim, "Dead-time compensation of current controlled inverter using the space vector method, " *Power Electronics and drive systems, Proceedings of 1995 International conference on*, 21-24 Feb. 1995, vol. 1, p 374-378

[36] IEC 61000-2-2:2002, "Electromagnetic compatibility (EMC), " Part 2: Environment, Section 2: Compatibility levels for low-frequency conducted disturbances and signaling in public low-voltage power supply systems, 2002

[37] IEC 61000-3-2:2000, "Electromagnetic compatibility (EMC), " Part 3: Limits, Section 2: Limits for harmonic current emissions (equipment input current ≤ 16 A per phase), 2000

[38] IEC 61000-3-4:1998, "Electromagnetic compatibility (EMC), " Part 3: Limits, Section 4: Limitation of emission of harmonic currents in low-voltage power supply systems for equipment with rated current greater than 16 A, 1998

[39] Michael J. Ryan, Robert D. Lorenz, Rik W. De Donker, "Modeling of multileg Sine-wave inverters: A Geometric Approach", *IEEE Transactions on Industry Applications*, Vol. 46, No 6, pp. 1183-1191, December 1999

[40] Michael J. Ryan, Rik W. De Donker, Robert D. Lorenz, "Decoupled Control of a Four-leg Inverter via a New 4 x 4 Transformation matrix", *IEEE Transactions on Power Electronics*, Vol. 16, No. 5, pp. 1183-1191, September 2002

[41] J.Y. Hung, W. Gao, J.C. Hung, "Variable structure control: A survey, "*IEEE Transactions on Industrial Electronics*, Vol. 40, No. 1, February 1993.

[42] V.I. Utkin, Sliding mode control design principles and applications to electric drives, "*IEEE Transactions on Industrial Electronics*, Vol. 40, No. 1, February 1993.

[43] S. Saetieo, R.Devaraj, D.A. Torrey, "The design and implementation of a three-phase active power filter based on sliding mode control, "*IEEE Transactions on Industry Applications*, Vol 31, No 5, pp. 993-1000, September/October 1995

[44] M. Carpita, M. Marchesoni, "Experimental Study of a power conditioning system using sliding mode control, " *IEEE Transactions on Power Electronics*, Vol. 11, No. 5, pp. 731-742, September 1996.

[45] N. Mendalek, K. Al-Haddad, F. Fnaiech, L.A. Dessaint, "Sliding mode control of a three-phase shunt active filter in the d-q frame, " *PESC'02*, Vol. 1, pp. 369-375, 2002

[46] B. Nicholas, M. Fadel, Y. Chéron, " Robust Control of switched Power converters via sliding Mode, " *ETEP*, vol. 6, no.6, pp. 413-418, November/December 1996

[47] M. Sedighy, S.B. Dewan, F.P. Dawson, " A robust Digital current control Method for active power filters, "*IEEE Transactions on Industry Applications*, Vol. 36, No. 4, pp. 1158-1164, July/August 2000

[48] W. Gao, J.C. Hung, "Variable structure Control of nonlinear Systems: A new Approach, "*IEEE Transactions on Industrial Electronics*, Vol. 40, No. 1, pp 45-55, February 1993.

Books

[H1] W.E. Kazibwe, M.H. Sendaula, "Electric Power Quality Control Techniques," Van Nostrand Reinhold, 1993

[H2] N. Mohan, T.M. Undeland, W.P. Robbins, "Power Electronics: Converters, Applications, and Design, Second Edition " John Wiley & Sons, Inc., 1995

[H3] W.H. Roadstrum, D.H. Wolaver, "Electrical Engineering for all engineers, " John Wiley & Sons, Inc., 1994

[H4] M.P. Kazmierkowski , R. Krishnan, F. Blaabjerg, "Control in Power electronics – Selected Problems, " Academic Press, 2002

[H5] G. F. Franklin, J. D. Powell, M. Workman, "Digital control of dynamic systems, Third Edition, " Addison Wesley Longman, Inc, 1998

[H6] D. A. Neamen, "Electronic circuit analysis and design, " The McGraw-Hill Companies, Inc, 1996

[H7] D.C. Lay, "Linear Algebra and its applications, Second Edition, "Addison Wesley Longman, Inc, 1997

[H8] V.I. Utkin, "Sliding modes in control Optimization, " Springer-Verlag Berlin, Heidelberg, 1992

[H9] C. Edwards, S.K. Spurgeon, "Sliding mode control: Theory and Applications, "Taylor & Francis Ltd, 1998

Appendix - Modelling and control of converters

A-1 Explanation of orthonormality in 3x3 transformation

1. By orthonormality is meant that:

$$\begin{aligned} I \bullet II &= \mathbf{0} \\ I \bullet III &= \mathbf{0} \\ II \bullet III &= \mathbf{0} \\ IV \bullet V &= \mathbf{0} \\ IV \bullet VI &= \mathbf{0} \\ V \bullet VI &= \mathbf{0} \end{aligned} \qquad \text{(A-1)}$$

Where I, II, III are respectively Column 1, Column 2 and Column 3 of the transformation matrix and IV, V, VI in turn represents the row vectors of the transformation matrix.

If a matrix complies with (A-1), it is orthogonal. For orthonormality the matrix must comply with the following additional criteria:

$$\begin{aligned} I \bullet I &= \mathbf{1} \\ II \bullet II &= \mathbf{1} \\ III \bullet III &= \mathbf{1} \\ IV \bullet IV &= \mathbf{1} \\ V \bullet V &= \mathbf{1} \\ VI \bullet VI &= \mathbf{1} \end{aligned} \qquad \text{(A-2)}$$

To comply with (A-2) the matrix must be multiplied by $\sqrt{\frac{2}{3}}$.

2. Representing the T_{qdo} matrix as

$$T_{dqo} = \sqrt{\frac{2}{3}} \begin{bmatrix} a & b & c \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}$$

The a, b and c column vectors are of equal magnitude and align with the phase vectors in the dq plane.

3. When a matrix T_{dqo} is orthonormal the inverse can easily be calculated: inverse(T_{dqo})=T_{dqo}^{T}.

A-2 Legend to explain numbering of sectors (not to scale)

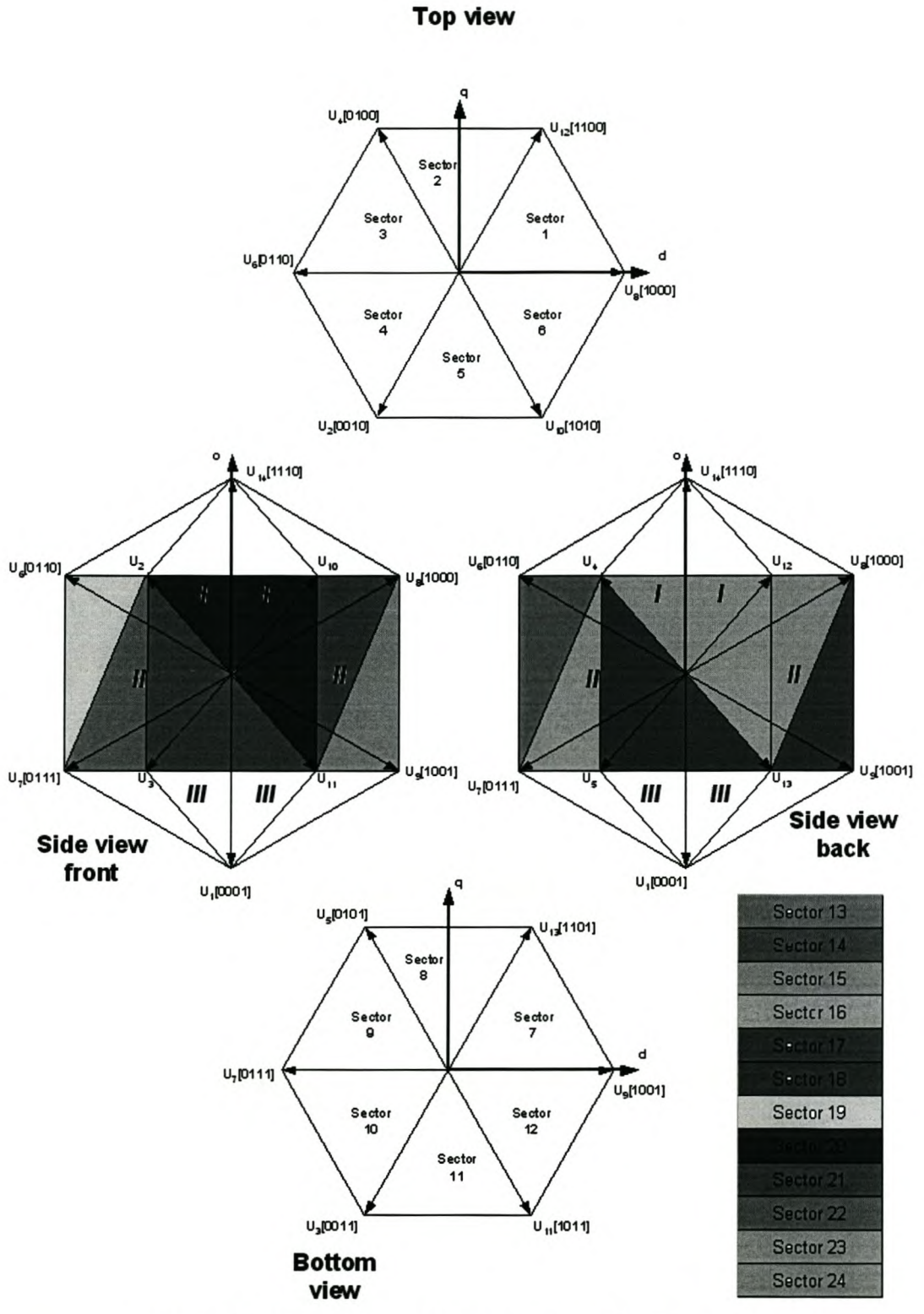


Figure A-1 Legend to explain numbering of sectors (not to scale)

A-3 List of inverse matrices for the different sectors

Table 24 - List of inverse matrices for the different sectors

Sector 1	$A^{-1} = \begin{bmatrix} 1.2247448 & -0.70710678 & 0 \\ 0 & 1.41421356 & 0 \\ -0.40824829 & -0.70710678 & 1.15470053 \end{bmatrix}$
Sector 2	$A^{-1} = \begin{bmatrix} -1.2247448 & 0.70710678 & 0 \\ 1.2247448 & 0.70710678 & 0 \\ -0.40824829 & -0.70710678 & 1.15470053 \end{bmatrix}$
Sector 3	$A^{-1} = \begin{bmatrix} 0 & 1.41421356 & 0 \\ -1.2247448 & -0.70710678 & 0 \\ 0.81649658 & 0 & 1.15470053 \end{bmatrix}$
Sector 4	$A^{-1} = \begin{bmatrix} 0 & -1.41421356 & 0 \\ -1.22474480 & 0.70710678 & 0 \\ 0.81649658 & 0 & 1.15470053 \end{bmatrix}$
Sector 5	$A^{-1} = \begin{bmatrix} -1.2247448 & -0.70710678 & 0 \\ 1.2247448 & -0.70710678 & 0 \\ -0.40824829 & 0.70710678 & 1.15470053 \end{bmatrix}$
Sector 6	$A^{-1} = \begin{bmatrix} 1.2247448 & 0.70710678 & 0 \\ 0 & -1.41421356 & 0 \\ -0.40824829 & 0.70710678 & 1.15470053 \end{bmatrix}$
Sector 7	$A^{-1} = \begin{bmatrix} -0.81649658 & 0 & -1.15470053 \\ 1.2247448 & -0.70710678 & 0 \\ 0 & 1.41421356 & 0 \end{bmatrix}$
Sector 8	$A^{-1} = \begin{bmatrix} 0.40824829 & -0.70710678 & -1.15470053 \\ -1.2247448 & 0.70710678 & 0 \\ 1.2247448 & 0.70710678 & 0 \end{bmatrix}$
Sector 9	$A^{-1} = \begin{bmatrix} 0.40824829 & -0.70710678 & -1.15470053 \\ 0 & 1.41421356 & 0 \\ -1.2247448 & -0.70710678 & 0 \end{bmatrix}$
Sector 10	$A^{-1} = \begin{bmatrix} 0.40824829 & 0.70710678 & -1.15470053 \\ 0 & -1.41421356 & 0 \\ -1.2247448 & 0.70710678 & 0 \end{bmatrix}$
Sector 11	$A^{-1} = \begin{bmatrix} 0.40824829 & 0.70710678 & -1.15470053 \\ -1.2247448 & -0.70710678 & 0 \\ 1.2247448 & -0.70710678 & 0 \end{bmatrix}$

Sector 12	$A^{-1} = \begin{bmatrix} -0.81649658 & 0 & -1.15470053 \\ 1.2247448 & 0.70710678 & 0 \\ 0 & -1.41421356 & 0 \end{bmatrix}$
Sector 13	$A^{-1} = \begin{bmatrix} -0.40824829 & -0.70710678 & 1.15470053 \\ 0.40824829 & -0.70710678 & -1.15470053 \\ -1.2247448 & 0.70710678 & 0 \end{bmatrix}$
Sector 14	$A^{-1} = \begin{bmatrix} -0.40824829 & -0.70710678 & 1.15470053 \\ -0.81649658 & 0 & -1.15470053 \\ 1.2247448 & -0.70710678 & 0 \end{bmatrix}$
Sector 15	$A^{-1} = \begin{bmatrix} 0.81649658 & 0 & 1.15470053 \\ 0.40824829 & 0.70710678 & -1.15470053 \\ 0 & -1.41421356 & 0 \end{bmatrix}$
Sector 16	$A^{-1} = \begin{bmatrix} -0.40824829 & 0.70710678 & 1.15470053 \\ 0.40824829 & 0.70710678 & -1.15470053 \\ -1.2247448 & -0.70710678 & 0 \end{bmatrix}$
Sector 17	$A^{-1} = \begin{bmatrix} -0.40824829 & 0.70710678 & 1.15470053 \\ -0.81649658 & 0 & -1.15470053 \\ 1.22474487 & 0.70710678 & 0 \end{bmatrix}$
Sector 18	$A^{-1} = \begin{bmatrix} 0.81649658 & 0 & 1.15470053 \\ 0.40824829 & -0.70710678 & -1.15470053 \\ 0 & 1.41421356 & 0 \end{bmatrix}$
Sector 19	$A^{-1} = \begin{bmatrix} 0 & -1.41421356 & 0 \\ -0.40824828 & 0.70710678 & 1.15470053 \\ -0.81649658 & 0 & -1.15470053 \end{bmatrix}$
Sector 20	$A^{-1} = \begin{bmatrix} -1.22474487 & -0.70710678 & 0 \\ 0.81649658 & 0 & 1.15470053 \\ 0.40824828 & -0.70710678 & -1.15470053 \end{bmatrix}$
Sector 21	$A^{-1} = \begin{bmatrix} 1.2247448 & 0.70710678 & 0 \\ -0.40824829 & -0.70710678 & 1.15470053 \\ 0.40824829 & -0.70710678 & -1.15470053 \end{bmatrix}$
Sector 22	$A^{-1} = \begin{bmatrix} 0 & 1.41421356 & 0 \\ -0.40824828 & -0.70710678 & 1.15470053 \\ -0.81649658 & 0 & -1.15470053 \end{bmatrix}$

Sector 23	$A^{-1} = \begin{bmatrix} -1.22474487 & 0.70710678 & 0 \\ 0.81649658 & 0 & 1.15470053 \\ 0.40824828 & 0.70710678 & -1.15470053 \end{bmatrix}$
Sector 24	$A^{-1} = \begin{bmatrix} 1.2247448 & -0.70710678 & 0 \\ -0.40824829 & 0.70710678 & 1.15470053 \\ 0.40824829 & 0.70710678 & -1.15470053 \end{bmatrix}$

A-4 Flowchart explaining process for determining the correct tetrahedron

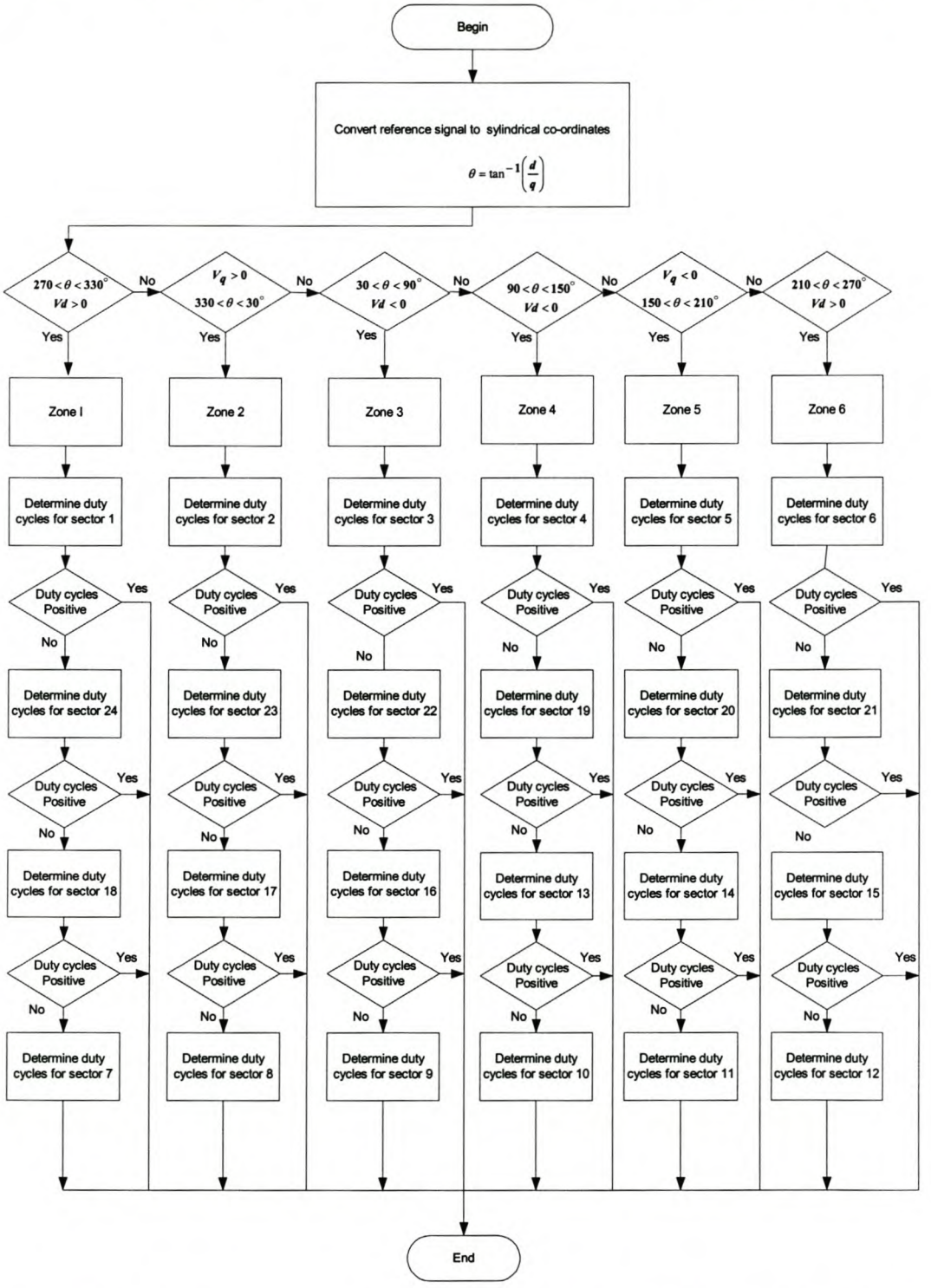


Figure 7-1- Flowchart explaining process for determining the correct tetrahedron

A-5 The optimum switching sequence for the different sectors

Table 25- The optimum switching sequence for the different sectors

Sector	States Involved	Optimum switching sequence
Sector 1	$U_8 - U_{12} - U_{14}$	0,8,12,14,15,14,12,8,0
Sector 2	$U_{12} - U_4 - U_{14}$	0,4,12,14,15,14,12,4,0
Sector 3	$U_4 - U_6 - U_{14}$	0,4,6,14,15,14,6,4,0
Sector 4	$U_6 - U_2 - U_{14}$	0,2,6,14,15,14,6,2,0
Sector 5	$U_2 - U_{10} - U_{14}$	0,2,10,14,15,14,10,2,0
Sector 6	$U_8 - U_{10} - U_{14}$	0,8,10,14,15,14,10,8,0
Sector 7	$U_9 - U_{13} - U_1$	0,1,9,13,15,13,9,1,0
Sector 8	$U_{13} - U_5 - U_1$	0,1,5,13,15,13,5,1,0
Sector 9	$U_5 - U_7 - U_1$	0,1,5,7,15,7,5,1,0
Sector 10	$U_7 - U_3 - U_1$	0,1,3,7,15,7,3,1,0
Sector 11	$U_3 - U_{11} - U_1$	0,1,3,11,15,11,3,1,0
Sector 12	$U_{11} - U_9 - U_1$	0,1,9,11,15,11,9,1,0
Sector 13	$U_7 - U_3 - U_2$	0,2,3,7,15,7,3,2,0
Sector 14	$U_{11} - U_3 - U_2$	0,2,3,11,15,11,3,2,0
Sector 15	$U_{11} - U_9 - U_8$	0,8,9,11,15,11,9,8,0
Sector 16	$U_7 - U_5 - U_4$	0,4,5,7,15,7,5,4,0
Sector 17	$U_5 - U_{13} - U_4$	0,4,5,13,15,13,5,4,0
Sector 18	$U_{13} - U_9 - U_8$	0,8,9,13,15,13,9,8,0
Sector 19	$U_6 - U_2 - U_7$	0,2,6,7,15,7,6,2,0
Sector 20	$U_2 - U_{10} - U_{11}$	0,2,10,11,15,11,10,2,0
Sector 21	$U_{10} - U_8 - U_{11}$	0,8,10,11,15,11,10,8,0
Sector 22	$U_6 - U_4 - U_7$	0,4,6,7,15,7,6,4,0
Sector 23	$U_4 - U_{12} - U_{13}$	0,4,12,13,15,13,12,4,0
Sector 24	$U_8 - U_{12} - U_{13}$	0,8,12,13,15,13,12,8,0

A-6 Duty cycles for the different phase arms when in a specific sector

Table 26 - Duty cycles for the different phase arms when in a specific sector

Sector 1	$D_A = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_3 + \frac{d_0}{2}$ $D_N = \frac{d_0}{2}$
Sector 2	$D_B = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_3 + \frac{d_0}{2}$ $D_N = \frac{d_0}{2}$
Sector 3	$D_B = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_3 + \frac{d_0}{2}$ $D_N = \frac{d_0}{2}$
Sector 4	$D_C = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_3 + \frac{d_0}{2}$ $D_N = \frac{d_0}{2}$
Sector 5	$D_C = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_3 + \frac{d_0}{2}$ $D_N = \frac{d_0}{2}$

Sector 6	$D_A = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_3 + \frac{d_0}{2}$ $D_N = \frac{d_0}{2}$
Sector 7	$D_N = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_3 + \frac{d_0}{2}$ $D_C = \frac{d_0}{2}$
Sector 8	$D_N = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_3 + \frac{d_0}{2}$ $D_C = \frac{d_0}{2}$
Sector 9	$D_N = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_3 + \frac{d_0}{2}$ $D_A = \frac{d_0}{2}$
Sector 10	$D_N = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_3 + \frac{d_0}{2}$ $D_A = \frac{d_0}{2}$

Sector 11	$D_N = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_3 + \frac{d_0}{2}$ $D_B = \frac{d_0}{2}$
Sector 12	$D_N = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_3 + \frac{d_0}{2}$ $D_B = \frac{d_0}{2}$
Sector 13	$D_C = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_3 + \frac{d_0}{2}$ $D_A = \frac{d_0}{2}$
Sector 14	$D_C = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_3 + \frac{d_0}{2}$ $D_B = \frac{d_0}{2}$
Sector 15	$D_A = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_3 + \frac{d_0}{2}$ $D_B = \frac{d_0}{2}$

Sector 16	$D_B = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_3 + \frac{d_0}{2}$ $D_A = \frac{d_0}{2}$
Sector 17	$D_B = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_3 + \frac{d_0}{2}$ $D_C = \frac{d_0}{2}$
Sector 18	$D_A = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_3 + \frac{d_0}{2}$ $D_C = \frac{d_0}{2}$
Sector 19	$D_C = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_3 + \frac{d_0}{2}$ $D_A = \frac{d_0}{2}$
Sector 20	$D_C = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_3 + \frac{d_0}{2}$ $D_B = \frac{d_0}{2}$

Sector 21	$D_A = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_3 + \frac{d_0}{2}$ $D_B = \frac{d_0}{2}$
Sector 22	$D_B = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_C = d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_3 + \frac{d_0}{2}$ $D_A = \frac{d_0}{2}$
Sector 23	$D_B = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_A = d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_3 + \frac{d_0}{2}$ $D_C = \frac{d_0}{2}$
Sector 24	$D_A = d_1 + d_2 + d_3 + \frac{d_0}{2}$ $D_B = d_2 + d_3 + \frac{d_0}{2}$ $D_N = d_3 + \frac{d_0}{2}$ $D_C = \frac{d_0}{2}$

Appendix B Proofs

B-1 Illustrating the orthogonal and parallel component of a vector onto another vector

Consider Figure B-1

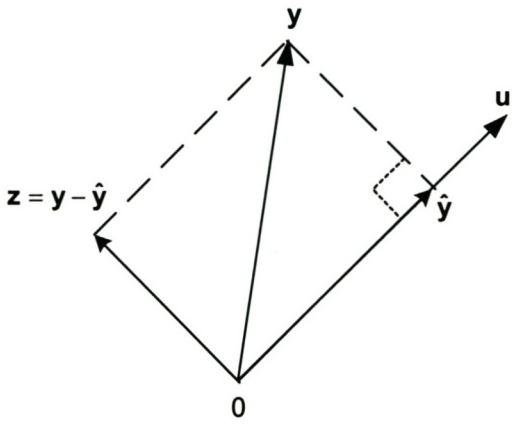


Figure B-1

From [H7] it can be found that the orthogonal projection of **y** onto **u** can be determined with:

$$\hat{\mathbf{y}} = \frac{\mathbf{y} \cdot \mathbf{u}}{\mathbf{u} \cdot \mathbf{u}} \mathbf{u}$$

, and the component of **y** orthogonal to **u** can be determined by using:

$$\mathbf{z} = \mathbf{y} - \frac{\mathbf{y} \cdot \mathbf{u}}{\mathbf{u} \cdot \mathbf{u}} \mathbf{u}$$

Appendix C Simulation and practical setup

C-1 Simulation and practical configuration

The simulation setup as shown in Figure C-1 is used to test the reference tracking performance of the current controllers without the neutral inductor connected.

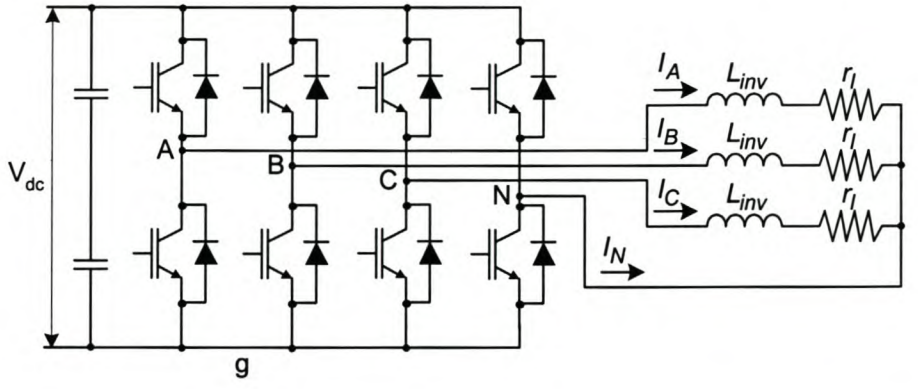


Figure C-1 – Current controller performance setup without neutral inductor

The simulation setup as shown in Figure C-2 is used to test the reference tracking performance of the current controllers without the neutral inductor connected.

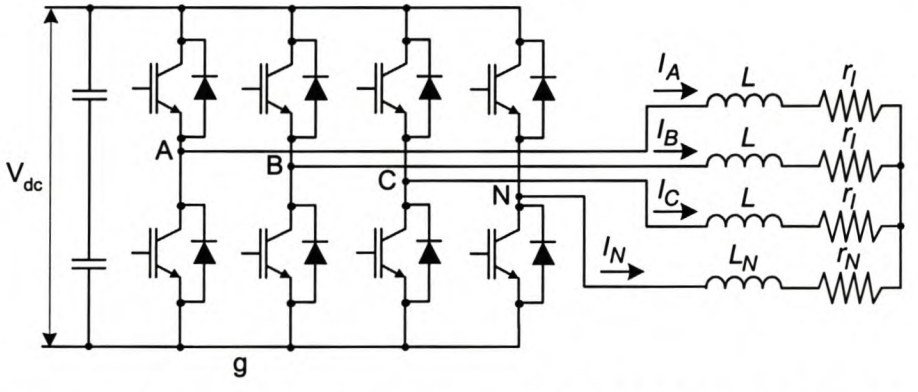


Figure C-2 Current controller performance setup with neutral inductor

The parameters used to test the performance of the current controllers is shown in Table 27

Table 27 Parameters used to test the current controllers

Parameter	Value
V_{dc}	800 V
L_{inv}	800 µH
L_N	800 µH
r_l	0.5 Ω
r_N	0.5 Ω
Switching sequence	Symmetrical aligned
Switching frequency	10 kHz
Dead-time	4.8uS

C-2 Simulation and practical configuration for shunt active power filter

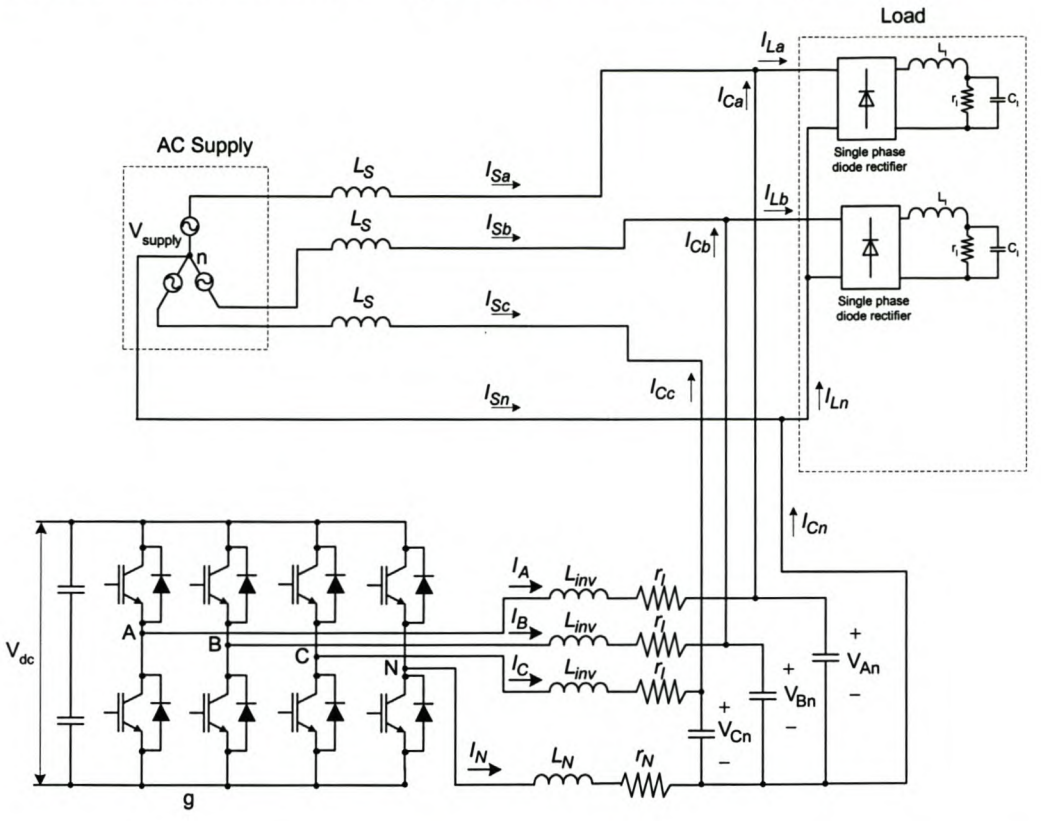


Figure C-3 Simulation and practical configuration for shunt active power filter

The parameters used to test the performance of the current controllers in a shunt active power application is shown in Table 28

Table 28 Parameters used to test the current controllers in a shunt active power filter

Parameter	Value
V_{dc}	800 V
L_{inv}	800 µH
L_N	800 µH
r_l	0.5 Ω
r_N	0.5 Ω
Filter capacitors	50 µF
Switching sequence	Symmetrical aligned
Switching frequency	10 kHz
Dead-time	4.8uS
L_S	100 µH
L_l	1.2 mH
r_l	3 Ω
C_l	3.3 mF

C-3 Practical setup for testing the three-dimensional space vector PWM

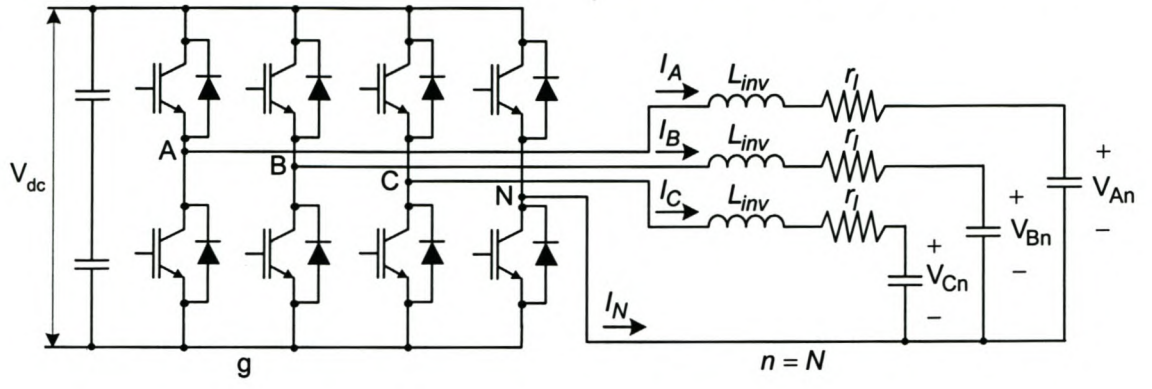


Figure C-4 Practical setup for testing the three-dimensional space vector PWM

The parameters used to test the performance of the current controllers is shown in Table 27

Table 29 Parameters used to test the current controllers

Parameter	Value
V_{dc}	800 V
L_{inv}	800 µH
L_N	800 µH
r_l	0.5 Ω
r_N	0.5 Ω
Filter capacitors	50 µF
Switching sequence	Symmetrical aligned
Switching frequency	10 kHz
Dead-time	4.8uS

Appendix D Source code

Code segment that transforms the line voltages and currents into the dq0 space

```
#ifndef _SPACE4
#define _SPACE4

#ifndef _INLINE
#error inline expansion of functions must be enabled (-x2)
#endif

#include "const.h"

/*4 phase transforms*/
#define Space4nid(Qa,Qb,Qc)    (0.81649658*(Qa) - 0.40824829*((Qb)+(Qc)))
#define Space4niq(Qa,Qb,Qc)          (0.70710678*((Qb)-(Qc)))
#define Space4ni0(Qa,Qb,Qc) (((Qa)+(Qb)+(Qc))*(1.15470054))

#define Space4nvd(Qa,Qb,Qc)    (0.81649658*(Qa) - 0.40824829*((Qb)+(Qc)))
#define Space4nvq(Qa,Qb,Qc)          (0.70710678*((Qb)-(Qc)))
#define Space4nv0(Qa,Qb,Qc) (((Qa)+(Qb)+(Qc))*(0.288675134))

/* Calculate the inverse of the 4 phase dq0z transform  */
#define Space4nia(Qd,Qq,Qo)    ((0.81649658*(Qd)) + (0.288675134*(Qo)))
#define Space4nib(Qd,Qq,Qo)          (((-0.40824829)*(Qd)) + (0.70710678*(Qq))+(0.288675134*(Qo)))
#define Space4nic(Qd,Qq,Qo) (((-0.40824829)*(Qd)) - (0.70710678*(Qq))+(0.288675134*(Qo)))
#define Space4nin(Qd,Qq,Qo) ((Qo)*(-0.866))

extern double  r_Vd, r_Vq, r_Vo;
extern double  mVdc;
extern double  imVdc;
extern double  s_Da, s_Db, s_Dc, s_Dn;
extern double  D0, D1, D2, D3;

void SpaceVectorPWM(void);

#endif
```

Three-dimensional space vector PWM code segment

```
#include "id.h"
#define FileID space_c



#include "space4.h"
#include "fpga.h"



double  D0, D1, D2, D3;
double  s_Da, s_Db, s_Dc, s_Dn;
double  s_Vd, s_Vq, r_Vd, r_Vq, r_Vo;
double k1d,k2d,k3d,k1q,k2q,k3q,k1o,k2o,k3o;


 /*_____Zone 1_____*/
 /* This code segment determine the duty cycles and limit the reference vector when  */
 /* necessary if the sector is in zone 1                                             */
```

```
static inline void CalcSector1()
{
 double       iD;

 D3 = imVdc*((-k1d)+(-k1q)+(k1o)  );          /*  Sector 1 */
 D2 = imVdc*((k2q)  );                       /*  Sector 1 */
 D1 = imVdc*((k2d)+(-k1q) );                 /*  Sector 1 */

 if ((D3>=0) && (D2>=0) && (D1>=0))          /*Determine if in sector 1*/
 {
  iD = (1.0)/(D1+D2+D3);   /* Determine if reference vector is in Linear region  */

 if (iD<1.0)
  {
   D3 *= iD;
   D2 *= iD;
   D1 *= iD;
   D0  = 0.0;                    /*  Delta 0 - Over modulation   */
   /*Calculating reference vector after limiting */
   r_Vd = mVdc*((D1*0.81649658)+(D2*0.40824829));
   r_Vq = mVdc*(D2*0.70710678);
   r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*0.866));
  }
 else
  {
   D0 = 0.5*(1.0-D1-D2-D3);          /*  Delta 0 - Linear region  */
  }
     s_Dn = D0;
     s_Dc = D3+s_Dn;
     s_Db = D2+s_Dc;
     s_Da = D1+s_Db;
}
else
{    D3 = -D3;                                 /*  Sector 24 */
     D2 = imVdc*((-k1d)+(k1q)+(k1o)  );        /*  Sector 24 */

     if ((D3>=0) && (D2>=0) && (D1>=0))         /*Determine if in sector 24*/
      {
       iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region  */

       if (iD<1.0)
        {
         D3 *= iD;
         D2 *= iD;
         D1 *= iD;
         D0  = 0.0;                  /*  Delta 0 - Over modulation   */
        /*Calculating reference vector after limiting */
         r_Vd = mVdc*((D1*0.81649658)+(D2*0.40824829)+(D3*0.40824829));
         r_Vq = mVdc*((D2*0.70710678)+(D3*0.70710678));
         r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*(-0.2887)));
        }
       else
        {
         D0 = 0.5*(1.0-D1-D2-D3);          /*  Delta 0 - Linear region  */
        }
       s_Dc = D0;
       s_Dn = D3+s_Dc;
       s_Db = D2+s_Dn;
       s_Da = D1+s_Db;
     }
```

```
        else
        { D3 = imVdc*((k2q)  );                    /* Sector 18 */
          D2 = -D2;                                /* Sector 18 */
          D1 = imVdc*((k3d)+(k1o) );               /* Sector 18 */

          if ((D3>=0) && (D2>=0) && (D1>=0))        /*Determine if in sector 18*/
           {
            iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

            if (iD<1.0)
             {
              D3 *= iD;
              D2 *= iD;
              D1 *= iD;
              D0  = 0.0;              /*  Delta 0 - Over modulation   */
              /*Calculating reference vector after limiting */
              r_Vd = mVdc*((D1*0.81649658)+(D2*0.8165)+(D3*0.40824829));
              r_Vq = mVdc*(D3*0.70710678);
              r_Vo = mVdc*((D1*0.2887)+(D2*(-0.5774))+(D3*(-0.2887)));
             }
            else
             {
              D0 = 0.5*(1.0-D1-D2-D3);      /*  Delta 0 - Linear region  */
             }
             s_Dc = D0;
             s_Db = D3+s_Dc;
             s_Dn = D2+s_Db;
             s_Da = D1+s_Dn;
           }
          else
           {D2 = imVdc*((k2d)+(-k1q)  );             /* Sector 7 */
            D1 = -D1;                                /* Sector 7 */

            iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

            if (iD<1.0)
             {
              D3 *= iD;
              D2 *= iD;
              D1 *= iD;
              D0  = 0.0;              /*  Delta 0 - Over modulation   */
              /*Calculating reference vector after limiting */
              r_Vd = mVdc*((D2*0.81649658)+(D3*0.40824829));
              r_Vq = mVdc*(D3*0.70710678);
              r_Vo = mVdc*((D1*(-0.866))+(D2*(-0.5774))+(D3*(-0.2887)));
             }
            else
             {
              D0 = 0.5*(1.0-D1-D2-D3);      /*  Delta 0 - Linear region  */
             }
              s_Dc = D0;
              s_Db = D3+s_Dc;
              s_Da = D2+s_Db;
              s_Dn = D1+s_Da;
             }

      }
   }

}
```

```
/*_____Zone 2_____*/
/* This code segment determine the duty cycles and limit the reference vector when  */
/* necessary if the sector is in zone 2                                             */
static inline void CalcSector2()
{
 double       iD;

 D3 = imVdc*((-k1d)+(-k1q)+(k1o)  );          /*  Sector 2 */
 D2 = imVdc*((k2d)+(k1q)  );                  /*  Sector 2 */
 D1 = imVdc*((-k2d)+(k1q) );                  /*  Sector 2 */

 if ((D3>=0) && (D2>=0) && (D1>=0))           /*Determine if in sector 2*/
  {
  iD = (1.0)/(D1+D2+D3);        /* Determine if reference vector is in Linear region */

    if (iD<1.0)
     {
      D3 *= iD;
      D2 *= iD;
      D1 *= iD;
      D0  = 0.0;                          /*  Delta 0 - Over modulation   */
     /*Calculating reference vector after limiting */
     r_Vd = mVdc*((D1*(-0.40824829))+(D2*0.40824829));
     r_Vq = mVdc*((D1*0.70710678)+(D2*0.70710678));
     r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*0.866));
    }
   else
    {
     D0 = 0.5*(1.0-D1-D2-D3);             /*  Delta 0 - Linear region  */
    }
  s_Dn = D0;
  s_Dc = D3+s_Dn;
  s_Da = D2+s_Dc;
  s_Db = D1+s_Da;
 }
else
 {
  D3 = -D3;                                /*  Sector 23 */
  D2 = imVdc*((k3d)+(k1o)  );              /*  Sector 23 */
  D1 = imVdc*((-k2d)+(k1q) );              /*  Sector 23 */

  if ((D3>=0) && (D2>=0) && (D1>=0))
    {
     iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

     if (iD<1.0)
       {
        D3 *= iD;
        D2 *= iD;
        D1 *= iD;
        D0  = 0.0;                  /*  Delta 0 - Over modulation   */
        /*Calculating reference vector after limiting */
        r_Vd = mVdc*((D1*(-0.40824829))+(D2*0.40824829)+(D3*0.40824829));
        r_Vq = mVdc*((D1*0.70710678)+(D2*0.70710678)+(D3*0.70710678));
        r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*(-0.2887)));
       }
      else
       {
        D0       = 0.5*(1.0-D1-D2-D3);    /*  Delta 0 - Linear region  */
```

```
 }
  s_Dc = D0;
  s_Dn = D3+s_Dc;
  s_Da = D2+s_Dn;
  s_Db = D1+s_Da;
 }
else
 { D3 = imVdc*((k2d)+(k1q)  );              /* Sector 17 */
   D2 = -D2;                                /* Sector 17 */
   D1 = imVdc*((-k1d)+(k1q)+(k1o) );        /* Sector 17 */

   if ((D3>=0) && (D2>=0) && (D1>=0))
    {
     iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

     if (iD<1.0)
      {
       D3 *= iD;
       D2 *= iD;
       D1 *= iD;
       D0  = 0.0;                 /*  Delta 0 - Over modulation   */
       /*Calculating reference vector after limiting */
       r_Vd = mVdc*((D1*(-0.40824829))+(D2*(-0.40824829))+(D3*0.40824829));
       r_Vq = mVdc*((D1*0.70710678)+(D2*0.70710678)+(D3*0.70710678));
       r_Vo = mVdc*((D1*0.2887)+(D2*(-0.5774))+(D3*(-0.2887)));
      }
     else
      {
       D0 = 0.5*(1.0-D1-D2-D3);         /*  Delta 0 - Linear region  */
      }
     s_Dc = D0;
     s_Da = D3+s_Dc;
     s_Dn = D2+s_Da;
     s_Db = D1+s_Dn;
     }
    else
     {D2 = imVdc*((-k2d)+(k1q)  );          /*  Sector 8 */
      D1 = -D1;                            /*  Sector 8 */

     iD =(1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

     if (iD<1.0)
      {
       D3 *= iD;
       D2 *= iD;
       D1 *= iD;
       D0  = 0.0;                 /*  Delta 0 - Over modulation   */
       /*Calculating reference vector after limiting */
       r_Vd = mVdc*((D2*(-0.40824829))+(D3*0.40824829));
       r_Vq = mVdc*((D2*0.70710678)+(D3*0.70710678));
       r_Vo = mVdc*((D1*(-0.866))+(D2*(-0.5774))+(D3*(-0.2887)));
      }
      else
      {
       D0       = 0.5*(1.0-D1-D2-D3);       /*  Delta 0 - Linear region  */
      }
     s_Dc = D0;
     s_Da = D3+s_Dc;
     s_Db = D2+s_Da;
     s_Dn = D1+s_Db;
```

```
            }

        }
    }

}

/*_____Zone 3_____*/
/* This code segment determine the duty cycles and limit the reference vector when  */
/* necessary if the sector is in zone 3                                             */

static inline void CalcSector3()
{
 double       iD;

 D3 = imVdc*((k3d)+(k1o)  );                /*  Sector 3 */
 D2 = imVdc*((-k2d)+(-k1q)  );              /*  Sector 3 */
 D1 = imVdc*((k2q) );                       /*  Sector 3 */


 if ((D3>=0) && (D2>=0) && (D1>=0))
  {
   iD = (1.0)/(D1+D2+D3);   /* Determine if reference vector is in Linear region */

      if (iD<1.0)
      {
       D3 *= iD;
       D2 *= iD;
       D1 *= iD;
       D0  = 0.0;                    /*  Delta 0 - Over modulation   */
       /*Calculating reference vector after limiting */
       r_Vd = mVdc*((D1*(-0.40824829))+(D2*(-0.81649658)));
       r_Vq = mVdc*(D1*0.70710678);
       r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*0.866));
      }
     else
      {
       D0 = 0.5*(1.0-D1-D2-D3);          /*  Delta 0 - Linear region  */
      }
   s_Dn = D0;
   s_Da = D3 + s_Dn;
   s_Dc = D2 + s_Da;
   s_Db = D1 + s_Dc;
 }
 else
  {
      D3 = -D3;                                    /*  Sector 22 */
      D2 = imVdc*((-k1d)+(-k1q)+(k1o)  );          /*  Sector 22 */
     if ((D3>=0) && (D2>=0) && (D1>=0))
       {
        iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

        if (iD<1.0)
         {
          D3 *= iD;
          D2 *= iD;
          D1 *= iD;
          D0  = 0.0;                    /*  Delta 0 - Over modulation   */
          /*Calculating reference vector after limiting */
```

```
        r_Vd = mVdc*((D1*(-0.40824829))+(D2*(-0.81649658))+(D3*(-0.81649658)));
        r_Vq = mVdc*(D1*0.70710678);
        r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*(-0.2887)));
        }
       else
        {
         D0 = 0.5*(1.0-D1-D2-D3);        /*  Delta 0 - Linear region  */
        }
       s_Da = D0;
       s_Dn = D3+s_Da;
       s_Dc = D2+s_Dn;
       s_Db = D1+s_Dc;
      }
    else
     { D3 = imVdc*((-k2d)+(-k1q)  );                /* Sector 16 */
       D2 = -D2;                                    /* Sector 16 */
       D1 = imVdc*((-k1d)+(k1q)+(k1o) );            /* Sector 16 */

       if ((D3>=0) && (D2>=0) && (D1>=0))
         {
          iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

          if (iD<1.0)
           {
            D3 *= iD;
            D2 *= iD;
            D1 *= iD;
            D0  = 0.0;              /*  Delta 0 - Over modulation   */
            /*Calculating reference vector after limiting */
            r_Vd = mVdc*((D1*(-0.40824829))+(D2*(-0.40824829))+(D3*(-0.81649658)));
            r_Vq = mVdc*((D1*0.70710678)+(D2*0.70710678));
            r_Vo = mVdc*((D1*0.2887)+(D2*(-0.5774))+(D3*(-0.2887)));
           }
          else
           {
            D0 = 0.5*(1.0-D1-D2-D3);        /*  Delta 0 - Linear region  */
           }
          s_Da = D0;
          s_Dc = D3+s_Da;
          s_Dn = D2+s_Dc;
          s_Db = D1+s_Dn;
         }
        else
         {D2 = imVdc*((k2q)  );                 /* Sector 9 */
          D1 = -D1;                             /* Sector 9 */

          iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

          if (iD<1.0)
           {
            D3 *= iD;
            D2 *= iD;
            D1 *= iD;
            D0  = 0.0;              /*  Delta 0 - Over modulation   */
            /*Calculating reference vector after limiting */
            r_Vd = mVdc*((D2*(-0.40824829))+(D3*(-0.81649658)));
            r_Vq = mVdc*(D2*0.70710678);
            r_Vo = mVdc*((D1*(-0.866))+(D2*(-0.5774))+(D3*(-0.2887)));
           }
          else
```

```
            {
             D0 = 0.5*(1.0-D1-D2-D3);       /* Delta 0 - Linear region */
            }
          s_Da = D0;
          s_Dc = D3+s_Da;
          s_Db = D2+s_Dc;
          s_Dn = D1+s_Db;
          }
        }

 }

}

/*_____________________________________________Slice 4_____________________________*/
/* This code segment determine the duty cycles and limit the reference vector when */
/* necessary if the sector is in zone 4                                            */

static inline void CalcSector4()
{
 double       iD;

 D3 = imVdc*((k3d)+(k1o) );                  /* Sector 4 */
 D2 = imVdc*((-k2d)+(k1q) );                 /* Sector 4 */
 D1 = imVdc*((-k2q) );                       /* Sector 4 */

 if ((D3>=0) && (D2>=0) && (D1>=0))
 {
  iD = (1.0)/(D1+D2+D3);   /* Determine if reference vector is in Linear region */
   if (iD<1.0)
     {
      D3 *= iD;
      D2 *= iD;
      D1 *= iD;
      D0  = 0.0;                  /* Delta 0 - Over modulation   */
      /*Calculating reference vector after limiting */
      r_Vd = mVdc*((D1*(-0.40824829))+(D2*(-0.81649658)));
      r_Vq = mVdc*(D1*(-0.70710678));
      r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*0.866));
     }
    else
     {
      D0       = 0.5*(1.0-D1-D2-D3);       /* Delta 0 - Linear region  */
     }
         s_Dn = D0;
         s_Da = D3+s_Dn;
         s_Db = D2+s_Da;
         s_Dc = D1+s_Db;
 }
 else
 {
     D3 = -D3;                                    /* Sector 19 */
     D2 = imVdc*((-k1d)+(k1q)+(k1o) );            /* Sector 19 */

      if ((D3>=0) && (D2>=0) && (D1>=0))
       {
        iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */
        if (iD<1.0)
          {
           D3 *= iD;
```

```
        D2 *= iD;
        D1 *= iD;
        D0  = 0.0;                  /*  Delta 0 - Over modulation   */
        /*Calculating reference vector after limiting */
        r_Vd = mVdc*((D1*(-0.40824829))+(D2*(-0.81649658))+(D3*(-0.81649658)));
        r_Vq = mVdc*(D1*(-0.70710678));
        r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*(-0.2887)));
        }
      else
        {
         D0 = 0.5*(1.0-D1-D2-D3);           /*  Delta 0 - Linear region  */
        }
      s_Da = D0;
      s_Dn = D3+s_Da;
      s_Db = D2+s_Dn;
      s_Dc = D1+s_Db;
     }
   else
     { D3 = imVdc*((-k2d)+(k1q)  );                 /* Sector 13  */
       D2 = -D2;                                   /* Sector 13  */
       D1 = imVdc*((-k1d)+(-k1q)+(k1o) );          /* Sector 13  */

      if ((D3>=0) && (D2>=0) && (D1>=0))
        {
           iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */
         if (iD<1.0)
           {
            D3 *= iD;
            D2 *= iD;
            D1 *= iD;
            D0  = 0.0;              /*  Delta 0 - Over modulation   */
            /*Calculating reference vector after limiting */
            r_Vd = mVdc*((D1*(-0.40824829))+(D2*(-0.40824829))+(D3*(-0.81649658)));
            r_Vq = mVdc*((D1*(-0.70710678))+(D2*(-0.70710678)));
            r_Vo = mVdc*((D1*0.2887)+(D2*(-0.5774))+(D3*(-0.2887)));
           }
         else
           {
            D0 = 0.5*(1.0-D1-D2-D3);       /*  Delta 0 - Linear region  */
           }
        s_Da = D0;
        s_Db = D3+s_Da;
        s_Dn = D2+s_Db;
        s_Dc = D1+s_Dn;
        }
      else
        {D2 = imVdc*((-k2q)  );                  /*  Sector10  */
         D1 = -D1;                               /*  Sector 10 */

        iD = (1.0)/(D1+D2+D3);  /* Determine if reference vector is in Linear region */
        if (iD<1.0)
         {
          D3 *= iD;
          D2 *= iD;
          D1 *= iD;
          D0  = 0.0;                  /*  Delta 0 - Over modulation   */
          /*Calculating reference vector after limiting */
          r_Vd = mVdc*((D2*(-0.40824829))+(D3*(-0.81649658)));
          r_Vq = mVdc*(D2*(-0.70710678));
          r_Vo = mVdc*((D1*(-0.866))+(D2*(-0.5774))+(D3*(-0.2887)));
```

```
            }
           else
            {
             D0 = 0.5*(1.0-D1-D2-D3);     /*  Delta 0 - Linear region  */
            }

            s_Da = D0;
            s_Db = D3+s_Da;
            s_Dc = D2+s_Db;
            s_Dn = D1+s_Dc;
           }

      }
 }

}

/*_____________________________________________Zone 5_____________________________________________*/
/* This code segment determine the duty cycles and limit the reference vector when  */
/* necessary if the sector is in zone 5                                             */

static inline void CalcSector5()
{
 double       iD;

 D3 = imVdc*((-k1d)+(k1q)+(k1o)  );          /*  Sector 5*/
 D2 = imVdc*((k2d)+(-k1q)  );                /*  Sector 5 */
 D1 = imVdc*((-k2d)+(-k1q) );                /*  Sector 5 */


 if ((D3>=0) && (D2>=0) && (D1>=0))
 {
  iD = (1.0)/(D1+D2+D3);          /* Determine if reference vector is in Linear region */
    if (iD<1.0)
     {
       D3 *= iD;
       D2 *= iD;
       D1 *= iD;
       D0  = 0.0;                 /*  Delta 0 - Over modulation   */
       /*Calculating reference vector after limiting */
       r_Vd = mVdc*((D1*(-0.40824829))+(D2*0.40824829));
       r_Vq = mVdc*((D1*(-0.70710678))+(D2*(-0.70710678)));
       r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*0.866));
     }
    else
     {
       D0 = 0.5*(1.0-D1-D2-D3);          /*  Delta 0 - Linear region  */
     }
         s_Dn = D0;
         s_Db = D3+s_Dn;
         s_Da = D2+s_Db;
         s_Dc = D1+s_Da;
 }
 else
 {
     D3 = -D3;                                  /* Sector 20  */
     D2 = imVdc*((k3d)+(k1o)  );                /* Sector 20 */
     if ((D3>=0) && (D2>=0) && (D1>=0))
       {
         iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */
```

```
if (iD<1.0)
    {
    D3 *= iD;
    D2 *= iD;
    D1 *= iD;
    D0  = 0.0;                  /*  Delta 0 - Over modulation   */
    /*Calculating reference vector after limiting */
    r_Vd = mVdc*((D1*(-0.40824829))+(D2*0.40824829)+(D3*0.40824829));
    r_Vq = mVdc*((D1*(-0.70710678))+(D2*(-0.70710678))+(D3*(-0.70710678)));
    r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*(-0.2887)));
    }
   else
    {
     D0 = 0.5*(1.0-D1-D2-D3);       /*  Delta 0 - Linear region  */
    }
   s_Db = D0;
   s_Dn = D3+s_Db;
   s_Da = D2+s_Dn;
   s_Dc = D1+s_Da;
  }
else
  { D3 = imVdc*((k2d)+(-k1q)  );                /*  Sector 14 */
    D2 = -D2;                                  /*  Sector 14 */
    D1 = imVdc*((-k1d)+(-k1q)+(k1o) );         /*  Sector 14 */
    if ((D3>=0) && (D2>=0) && (D1>=0))
      {
        iD  = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

        if (iD<1.0)
         {
          D3 *= iD;
          D2 *= iD;
          D1 *= iD;
          D0  = 0.0;            /*  Delta 0 - Over modulation   */
          /*Calculating reference vector after limiting */
          r_Vd = mVdc*((D1*(-0.40824829))+(D2*(-0.40824829))+(D3*0.40824829));
          r_Vq = mVdc*((D1*(-0.70710678))+(D2*(-0.70710678))+(D3*(-0.70710678)));
          r_Vo = mVdc*((D1*0.2887)+(D2*(-0.5774))+(D3*(-0.2887)));
         }
        else
         {
          D0 = 0.5*(1.0-D1-D2-D3);   /*  Delta 0 - Linear region  */
         }
       s_Db = D0;
       s_Da = D3+s_Db;
       s_Dn = D2+s_Da;
       s_Dc = D1+s_Dn;
       }
     else
       {D2 = imVdc*((-k2d)+(-k1q)  );          /*  Sector 11 */
        D1 = -D1;                             /*  Sector 11 */


       iD  = (1.0)/(D1+D2+D3);      /* Determine if reference vector is in Linear region */

       if (iD<1.0)
        {
         D3 *= iD;
         D2 *= iD;
         D1 *= iD;
```

```
            D0  = 0.0;              /*  Delta 0 - Over modulation   */
            /*Calculating reference vector after limiting */
            r_Vd = mVdc*((D2*(-0.40824829))+(D3*0.40824829));
            r_Vq = mVdc*((D2*(-0.70710678))+(D3*(-0.70710678)));
            r_Vo = mVdc*((D1*(-0.866))+(D2*(-0.5774))+(D3*(-0.2887)));
           }
          else
           {
            D0 = 0.5*(1.0-D1-D2-D3);      /*  Delta 0 - Linear region  */
           }

        s_Db = D0;
        s_Da = D3+s_Db;
        s_Dc = D2+s_Da;
        s_Dn = D1+s_Dc;
          }

      }
 }

}


/*_____________________________________________Zone 6_____________________________________________*/
/* This code segment determine the duty cycles and limit the reference vector when  */
/* necessary if the sector is in zone 6                                             */

static inline void CalcSector6()
{
 double       iD;

 D3 = imVdc*((-k1d)+(k1q)+(k1o)  );              /*  Sector 6 */
 D2 = imVdc*((-k2q)  );                          /*  Sector 6 */
 D1 = imVdc*((k2d)+(k1q) );                      /*  Sector 6 */


 if ((D3>=0) && (D2>=0) && (D1>=0))
 {
  iD = (1.0)/(D1+D2+D3);     /* Determine if reference vector is in Linear region */

   if (iD<1.0)
    {
     D3 *= iD;
     D2 *= iD;
     D1 *= iD;
     D0  = 0.0;                    /*  Delta 0 - Over modulation   */
     /*Calculating reference vector after limiting */
     r_Vd = mVdc*((D1*0.81649658)+(D2*0.40824829));
     r_Vq = mVdc*(D2*(-0.70710678));
     r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*0.866));
    }
   else
    {
     D0 = 0.5*(1.0-D1-D2-D3);          /*  Delta 0 - Linear region  */
    }
       s_Dn = D0;
       s_Db = D3+s_Dn;
       s_Dc = D2+s_Db;
       s_Da = D1+s_Dc;
 }
```

```
else
{
    D3 = -D3;                                   /* Sector 21 */
    D2 = imVdc*((-k1d)+(-k1q)+(k1o)  );         /* Sector 21 */

    if ((D3>=0) && (D2>=0) && (D1>=0))
      {
       iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

       if (iD<1.0)
        {
        D3 *= iD;
        D2 *= iD;
        D1 *= iD;
        D0  = 0.0;                      /*  Delta 0 - Over modulation   */
        /*Calculating reference vector after limiting */
        r_Vd = mVdc*((D1*0.81649658)+(D2*0.40824829)+(D3*0.40824829));
        r_Vq = mVdc*((D2*(-0.70710678))+(D3*(-0.70710678)));
        r_Vo = mVdc*((D1*0.2887)+(D2*0.5774)+(D3*(-0.2887)));
        }
       else
        {
         D0 = 0.5*(1.0-D1-D2-D3);           /*  Delta 0 - Linear region  */
        }
       s_Db = D0;
       s_Dn = D3+s_Db;
       s_Dc = D2+s_Dn;
       s_Da = D1+s_Dc;
      }
    else
      { D3 = imVdc*((-k2q)  );                  /*  Sector 15 */
        D2 = -D2;                               /*  Sector 15 */
        D1 = imVdc*((k3d)+(k1o) );              /*  Sector 15 */
        if ((D3>=0) && (D2>=0) && (D1>=0))
          {
           iD = (1.0)/(D1+D2+D3);     /* Determine if reference vector is in Linear region */

           if (iD<1.0)
            {
             D3 *= iD;
             D2 *= iD;
             D1 *= iD;
             D0  = 0.0;                 /*  Delta 0 - Over modulation   */
             /*Calculating reference vector after limiting */
             r_Vd = mVdc*((D1*0.81649658)+(D2*0.81649658)+(D3*0.40824829));
             r_Vq = mVdc*((D3*(-0.70710678)));
             r_Vo = mVdc*((D1*0.2887)+(D2*(-0.5774))+(D3*(-0.2887)));
            }
           else
            {
             D0  = 0.5*(1.0-D1-D2-D3);    /*  Delta 0 - Linear region  */
            }
           s_Db = D0;
           s_Dc = D3+s_Db;
           s_Dn = D2+s_Dc;
           s_Da = D1+s_Dn;
          }
         else
          {
           D2 = imVdc*((k2d)+(k1q)  );          /* Sector 12 */
```

```
            D1 = -D1;                                   /* Sector 12 */

            iD = (1.0)/(D1+D2+D3); /* Determine if reference vector is in Linear region */

            if (iD<1.0)
             {
              D3 *= iD;
              D2 *= iD;
              D1 *= iD;
              D0  = 0.0;                /*  Delta 0 - Over modulation   */
              /*Calculating reference vector after limiting */
              r_Vd = mVdc*((D2*0.81649658)+(D3*0.40824829));
              r_Vq = mVdc*((D3*(-0.70710678)));
              r_Vo = mVdc*((D1*(-0.866))+(D2*(-0.5774))+(D3*(-0.2887)));
             }
            else
             {
              D0 = 0.5*(1.0-D1-D2-D3);       /*  Delta 0 - Linear region  */
             }

          s_Db = D0;
          s_Dc = D3+s_Db;
          s_Da = D2+s_Dc;
          s_Dn = D1+s_Da;
            }

        }
   }

 }

/*_____________________________________________space vector duty-cycle_______*/
void SpaceVectorPWM()
{

k1d = r_Vd*0.40824829;
k2d = r_Vd*1.22474487;
k3d = r_Vd*0.81649658;

k1q = r_Vq*0.70710678;
k2q = r_Vq*1.41421356;

k1o = r_Vo*1.15470053;


 /*.....................................................determine Zone.....................*/
 if (r_Vq>=0)
 {
  /*.....................................................Zone 1/2/3.....................*/
  if (r_Vq>(1.732*fabs(r_Vd)))
    CalcSector2();                                      /*  Zone 2          */
  else
  {
    if (r_Vd<0)
      CalcSector3();                                    /*  Zone 3          */
    else
      CalcSector1();                                    /*  Zone 1          */
  }
 }
 else
```

```
  {
   /*.....Zone 4/5/6.....*/
   if (r_Vq<(-1.732*fabs(r_Vd)))
     CalcSector5();                          /* Zone 5      */
   else
   {
     if (r_Vd<0)
       CalcSector4();                        /* Zone 4      */
     else
       CalcSector6();                        /* Zone 6      */
   }
  }
}
```

Code segment that is doing the basic calculations

```
#include "id.h"
#define FileID modec_c


#include "modec.h"
#include "supply.h"
#include "space4.h"


double wtu  = 0;
double wtu1 = 0;     /* Set to 333 when testing current control in a star connection*/
double wtu2 = 666;
double coswts, sinwts;
double coswtu, sinwtu;
double coswtu1, sinwtu1;
double Il_a, cAPF;
double r_Vdc;
double rIfd, rIfq;
double zmIld, zmIlq;
double start_flag =0;
double start_flag1 =0;
double I_pred_d, I_pred_q, I_pred_0;
double rIfdold = 0.0;
double rIfqold = 0.0;
double rIf0old = 0.0;

double cUPS;

double mVdc;
double imVdc;
double mVbat;

double mVsd, mVsq, mVs, imVs;
double mVfd, mVfq,mVf0, mVf_2,imVf_2;
double mIsd, mIsq, mIs0, mIs_2;
double mIld, mIlq, mIl0, mIl_2;
double mIfd, mIfq, mIf0, mIf_2;

double f_mVf_2 = 0.0;

double f_mIs_2 = 0.0;
```

```
double f_mIf_2 = 0.0;
double f_mIl_2 = 0.0;

double f_mIs0_2 = 0.0;
double f_mIf0_2 = 0.0;
double f_mIl0_2 = 0.0;
double On_off_toggle = 0.0;

double mVf, imVf;
double coswtf, sinwtf;
double  Iacheck,Ibcheck,Iccheck,Incheck;

/*_____________________________________________________*/

/* new pointer with reference to __sin1k tables -JAD */
const double * const sin1k = _sin1k;
const double * const cos1k = _cos1k;

/*_____________________________________________________*/

/* WS 15-02-2003: Add. */
#if SINGLE_P_TRIP
double f_s_Isa = 0.0;
double f_s_Isb = 0.0;
double f_s_Isc = 0.0;
double f_s_Ifa = 0.0;
double f_s_Ifb = 0.0;
double f_s_Ifc = 0.0;
double f_s_Ila = 0.0;
double f_s_Ilb = 0.0;
double f_s_Ilc = 0.0;
double f_s_Ibat = 0.0;
#endif

/*_____________________________________________________________________________*/

void CalcBasic(double d_wtu)
{
   double Ifa1, Ifb1, Ifc1, Vfa1, Vfb1, Vfc1, Ila1, Ilb1, Ilc1;

 /*Change the measured values to actual volts and currents*/
Ifa1 = ADC->Ifa*cDI;
Ifb1 = ADC->Ifb*cDI;
Ifc1 = ADC->Ifc*cDI;

Vfa1 = ADC->Vfa*cDV;
Vfb1 = ADC->Vfb*cDV;
Vfc1 = ADC->Vfc*cDV;

Ila1 = ADC->Ila*cDI;
Ilb1 = ADC->Ilb*cDI;
Ilc1 = ADC->Ilc*cDI;


 /*  filter voltage  */
 mVfd     = Space4nvd(Vfa1,Vfb1,Vfc1);
 mVfq     = Space4nvq(Vfa1,Vfb1,Vfc1);
 mVf0     = Space4nv0(Vfa1,Vfb1,Vfc1);

 /*  load current  */
```

```
  mIId     = Space4nid(Ila1,Ilb1,Ilc1);
  mIIq     = Space4niq(Ila1,Ilb1,Ilc1);
  mII0     = Space4ni0(Ila1,Ilb1,Ilc1);

  /* filter current */
  mIfd     = Space4nid(Ifa1,Ifb1,Ifc1);
  mIfq     = Space4niq(Ifa1,Ifb1,Ifc1);
  mIf0     = Space4ni0(Ifa1,Ifb1,Ifc1);

  /* dc-bus voltage */
  mVdc     = ADC->Vdh-ADC->Vdl;
  mVdc = mVdc*cDV;
  if (mVdc<1.0)  mVdc  = 1.0;
    imVdc    = (1.0)/mVdc;

/* Magnitude of the filter Voltage in the dq plane */
   mVf = max(1.0,sqrt((mVfd*mVfd)+(mVfq*mVfq)));
   imVf     = (1.0)/mVf;

/* Magnitude of the filter Voltage in the dq0 space */
  mVf_2    = max(1.0,((mVfd*mVfd)+(mVfq*mVfq)+(mVf0*mVf0)));
  imVf_2   = (1.0)/mVf_2;

/* Filtered magnitude of the filter Voltage in the dq0 space */
  f_mVf_2  += 0.5*(mVf_2-f_mVf_2);

/* Phase lock loop */

  coswtf   = imVf*mVfd;              /* x-comp */
  sinwtf   = imVf*mVfq;              /* y-comp */

 wtu      += 5; /* Sampling frequency=10 kHz(1000 sample points)*(50Hz period/Sampling frequency)*/

   if (((coswtf*coswtu)+(sinwtf*sinwtu))<0.0)
    {
     wtu += 0.25;
    }
   else
    {
     wtu -= 0.25;
    }

 /* limit wtu */
  if (wtu<0.0)          wtu  += 1000.0;
  if (wtu>=1000.0)      wtu  -= 1000.0;

  wtu1      = wtu;
  wtu1      += 245;

  /* limit wtu1 */
  if (wtu1<0.0)         wtu1  += 1000.0;
  if (wtu1>=1000.0)     wtu1  -= 1000.0;

  coswtu   = cos1k[(int)(wtu)];
  sinwtu   = sin1k[(int)(wtu)];

  coswtu1   = cos1k[(int)(wtu1)];
  sinwtu1   = sin1k[(int)(wtu1)];
}
```

Code segment that generate the reference voltages

```
#ifndef __modec
#define __modec

#ifndef _INLINE
#error inline expansion of functions must be enabled (-x2)
#endif


#include <float.h>
#include <math.h>
#include "adc.h"
#include "parm.h"
#include "macro.h"
#include "space4.h"
#include "supply.h"
#include "..\shared\source\options.h"
#include "fpga.h"


extern double  r_Vdc;
extern double  Il_a, cAPF;
extern double  mVsd, mVsq, mVs, imVs;
extern double  mVfd, mVfq,mVf0,mVf_2;
extern double  mIsd, mIsq, mIs0, mIs_2;
extern double  mIld, mIlq, mIl0, mIl_2;
extern double  mIfd, mIfq, mIf0, mIf_2;
extern double  mVbat;
extern double  mVdc;
extern double  coswts, sinwts;
extern double  coswtu, sinwtu;
extern double  coswtu1, sinwtu1;
extern double  wtu,wtu1,wtu2;
extern double  cUPS;
extern double  Iacheck,Ibcheck,Iccheck,Incheck;

/*_____________________________________________________*/

/* new pointer with reference to __sin1k tables -JAD */
/*extern const double  cos1k[], sin1k[];*/
extern const double _cos1k[], _sin1k[];
extern const double * const sin1k;
extern const double * const cos1k;

void CalcBasic(double d_wtu);

/*_____________________________________________________*/

/*extern const double  cos1k[], sin1k[];*/

extern double zmIld, zmIlq;
extern double f_mVf_2;
extern double f_mIs_2, f_mIl_2, f_mIf_2;
extern double f_mIs0_2, f_mIl0_2, f_mIf0_2;
extern double start_flag,start_flag1;
extern double I_pred_d, I_pred_q, I_pred_0,rIfdold,rIfqold,rIf0old;
extern double Irefout, Irefold,Vdifffiltered, Vdiff1, Vdifffiltered2,Vdifffiltered1,Vdiff2,Vdiff;
extern double I_drot_ref, I_qrot_ref, Idfiltered,Idfiltered1,Idfiltered2,I_drot_ref1,I_drot_ref2;
```

```
extern double I_Dac, I_Qac,current_scalefactor,On_off_toggle;
extern double mVf, imVf;
extern double coswtf, sinwtf;


extern type_ADCfile*        dprADCfile;

static inline void CalcAPFref()
{
  double rlfd, rlfq, rlf0, V_deq, V_qeq, V_oeq, alphaD, alphaQ, alphazero, xdot1, xdot2, xdot3;
  double alphaDsignum, alphaQsignum, alphazerosignum;
  double V_D,I_Dac_applied,I_Qac_applied;
  double V_Q;
  double V_O;

/* Regulation of the DC bus  */

Vdiff= 790.0-mVdc;          /* Reference DC bus voltage is set to 790 V */

/* 2nd order Butterworth low pass filter with 3 dB cuttoff frequency of 20 Hz */
Vdifffiltered=(1.982*Vdifffiltered1)-(0.9824*Vdifffiltered2)+(78.51e-6*Vdiff1)+(78.51e-6*Vdiff2);

/* PI controller used to regulate the DC BUS voltage*/
Irefout=0.5*(Irefold+(1.0*Vdifffiltered));

Vdifffiltered2=Vdifffiltered1;
Vdifffiltered1=Vdifffiltered;
Vdiff2=Vdiff1;
Vdiff1=Vdiff;

/*Limit Irefout */

if (Irefout>=50.0)
   {
    Irefout=50.0;
    Irefold=Irefout;
   }
else if (Irefout<=-50.0)
    {
     Irefout=-50.0;
     Irefold=Irefout;
    }
   else Irefold=Irefout;

 /* Synchronous reference method used to generate reference signal */
I_drot_ref=(mIId*coswtu1) + (mIIq*sinwtu1);
I_qrot_ref=((-sinwtu1)*mIId)+(coswtu1*mIIq);

/*Filter the DC component from I_drot_ref */
Idfiltered +=0.004*(I_drot_ref-Idfiltered);

I_Dac = I_drot_ref-Idfiltered;
I_Qac = I_qrot_ref;
I_Dac_applied = current_scalefactor*On_off_toggle*I_Dac; /*Ramped value*/
I_Qac_applied = current_scalefactor*On_off_toggle*I_Qac; /*Ramped value*/

/* Generate the reference vector in the Stationary dqo space */
 rlfd     = ((coswtu1*(I_Dac_applied-Irefout))+((-sinwtu1)*I_Qac_applied));
 rlfq     = ((sinwtu1*(I_Dac_applied-Irefout))+(coswtu1*I_Qac_applied));
 rlf0     = current_scalefactor*((On_off_toggle*mII0));
```

```
/* Convert reference current in dqo space back to the line currents  */
Iacheck= Space4nia(rlfd,rlfq,rlf0);
Ibcheck= Space4nib(rlfd,rlfq,rlf0);
Iccheck= Space4nic(rlfd,rlfq,rlf0);
Incheck= Space4nin(rlfd,rlfq,rlf0);

V_D = mVfd;
V_Q = mVfq;
V_O = mVf0;

/* Calculate the predicted current values */

I_pred_d= ((1-((Tsapf*Rinv)*iLinv))*mIfd)+((Tsapf*r_Vd)*iLinv)-((Tsapf*V_D)*iLinv);
I_pred_q= ((1-((Tsapf*Rinv)*iLinv))*mIfq)+((Tsapf*r_Vq)*iLinv)-((Tsapf*V_Q)*iLinv);
I_pred_0= ((1-
(Tsapf*((0.75*Rneutral)+(0.25*Rinv))/((0.75*Lneutral)+(0.25*Linv))))*mIf0)+((Tsapf*r_Vo)/((0.75*Lneutral)
+(0.25*Linv)))-((Tsapf*V_O)/((0.75*Lneutral)+(0.25*Linv)));

/* Calculate the voltage refererence needed for proper current regulation - using predicted currents */
/*
r_Vd = (((Linv/100e-6)*(rIfd-I_pred_d))+(Rinv*I_pred_d)+V_D);
r_Vq = (((Linv/100e-6)*(rIfq-I_pred_q))+(Rinv*I_pred_q)+V_Q);
r_Vo = (((((0.75*Lneutral)+(0.25*Linv))/100e-6)*(rIf0-
I_pred_0))+(((0.75*Rneutral)+(0.25*Rinv))*I_pred_0)+V_O);

*/
/* Calculate the voltage refererence needed for proper current regulation - using measured currents */
/*
r_Vd = (((Linv*10000)*(rIfd-mIfd))+(Rinv*mIfd)+V_D);
r_Vq = (((Linv*10000)*(rIfq-mIfq))+(Rinv*mIfq)+V_Q);
r_Vo = (((((0.75*Lneutral)+(0.25*Linv))*10000)*(rIf0-mIf0))+(((0.75*Rneutral)+(0.25*Rinv))*mIf0)+V_O);
*/

/* Sliding mode control - Equivalent control*/

xdot1=10000*(rIfd-rIfdold);
xdot2=10000*(rIfq-rIfqold);
xdot3=10000*(rIf0-rIf0old);

rIfdold=rIfd;
rIfqold=rIfq;
rIf0old=rIf0;

V_deq= (Rinv*I_pred_d)+V_D+(Linv*xdot1);
V_qeq= (Rinv*I_pred_q)+V_Q+(Linv*xdot2);
V_oeq = (((0.75*Rneutral)+(0.25*Rinv))*I_pred_0)+V_O+(((0.75*Lneutral)+(0.25*Linv))*xdot3);

/* Sliding mode control - Ideal saturation control*/
/*
alphaD=0.015*(rIfd-I_pred_d);
alphaQ=0.015*(rIfq-I_pred_q);
alphazero=0.00375*(rIf0-I_pred_0);  */
                    /*For sero sequence: Use 0.015 when 800uH neutral inductor connected, else*/
                    /*                   no neutral inductor connected use 0.00375 */
/*if (alphaD>1) alphaD=1;
if (alphaD<-1) alphaD=-1;

if (alphaQ>1) alphaQ=1;
if (alphaQ<-1) alphaQ=-1;
```

```
if (alphazero>1) alphazero=1;
if (alphazero<-1) alphazero=-1;

r_Vd = (V_deq) + (mVdc*alphaD);
r_Vq = (V_qeq) + (mVdc*alphaQ);
r_Vo = (V_oeq) + (mVdc*alphazero);
*/
/* Sliding mode control - constant rate*/
/*
alphaD=(rlfd-I_pred_d);
alphaQ=(rlfq-I_pred_q);
alphazero=(rlf0-I_pred_0);

alphaD = (alphaD>0.0?mVdc:-mVdc);
alphaQ = (alphaQ>0.0?mVdc:-mVdc);
alphazero = (alphazero>0.0?mVdc:-mVdc);

r_Vd = V_deq + (0.01*alphaD);
r_Vq = V_qeq + (0.01*alphaQ);
r_Vo = V_oeq + (0.0025*alphazero); */
                /*For sero sequence: Use 0.01 when 800uH neutral inductor connected, else*/
                /*              no neutral inductor connected use 0.0025 */

/* Sliding mode control - constant rate + proportional control*/

alphaD=(rlfd-I_pred_d);
alphaQ=(rlfq-I_pred_q);
alphazero=(rlf0-I_pred_0);

alphaDsignum = (alphaD>0.0?mVdc:-mVdc);
alphaQsignum = (alphaQ>0.0?mVdc:-mVdc);
alphazerosignum = (alphazero>0.0?mVdc:-mVdc);
r_Vd = V_deq + (0.003*alphaDsignum)+ (0.016*mVdc*alphaD);
r_Vq = V_qeq + (0.003*alphaQsignum)+ (0.016*mVdc*alphaQ);
r_Vo = V_oeq + (0.003*alphazerosignum)+ (0.016*mVdc*alphazero);
                /* For sero sequence: Use 0.003 and 0.016 when 800uH neutral inductor connected*/
                /*              no neutral inductor connected use 0.00075 and 0.004 */

/* Calcualte the respective phases duty cycle */
SpaceVectorPWM();    /* Duration: 15 us to execute  */
}
```

Code segment that compensate for dead-time effects

```
static inline void CalcAPFDead_time()
{

#define Te_dead (38e-3)  /*Dead time is set to 4.8uS */
                /* Ton = 0.2uS */
                /* Toff = 1.2uS */
                /* Te = (Dead Time + Ton)-Toff= 4.025 uS */
                /*Value that is going to the FPGA is Te/Switching period=40.25e-3 */


if ((s_Da > Te_dead)&&(s_Db > Te_dead)&&(s_Dc > Te_dead)&&(s_Dn > Te_dead))
 {/*Mode 1*/
```

```
 if (Iacheck>=0.0) s_Da=s_Da+Te_dead;
 else s_Da=s_Da-Te_dead;

/* Calculate dead_time compensation for Phase arm B */
 if (Ibcheck>=0.0) s_Db=s_Db+Te_dead;
 else s_Db=s_Db-Te_dead;

/* Calculate dead_time compensation for Phase arm C */
 if (Iccheck>=0.0) s_Dc=s_Dc+Te_dead;
 else s_Dc=s_Dc-Te_dead;

/* Calculate dead_time compensation for Phase arm N */
 if (Incheck>=0.0) s_Dn=s_Dn+Te_dead;
 else s_Dn=s_Dn-Te_dead;

}
/*Mode 2*/
 else if ((s_Da<=Te_dead)&&(Iacheck>=0.0))
     {
      if (Ibcheck<0.0) s_Db=s_Db-(s_Da-Te_dead);
      else  s_Db=s_Db-(s_Da+Te_dead);

      if (Iccheck<0.0) s_Dc=s_Dc-(s_Da-Te_dead);
      else  s_Dc=s_Dc-(s_Da+Te_dead);

      if (Incheck<0.0) s_Dn=s_Dn-(s_Da-Te_dead);
      else  s_Dn=s_Dn-(s_Da+Te_dead);
     }
  else if ((s_Da<=Te_dead)&&(Iacheck<0.0))
    {
      if (Ibcheck<0.0) s_Db=s_Db-(s_Da-Te_dead);
      else  s_Db=s_Db-(s_Da-(3.0*Te_dead));

      if (Iccheck<0.0) s_Dc=s_Dc-(s_Da-Te_dead);
      else  s_Dc=s_Dc-(s_Da-(3.0*Te_dead));

      if (Incheck<0.0) s_Dn=s_Dn-(s_Da-Te_dead);
      else  s_Dn=s_Dn-(s_Da-(3.0*Te_dead));
    }
 else if ((s_Db<=Te_dead)&&(Ibcheck>=0.0))
     {
      if (Iacheck<0.0) s_Da=s_Da-(s_Db-Te_dead);
      else  s_Da=s_Da-(s_Db+Te_dead);

      if (Iccheck<0.0) s_Dc=s_Dc-(s_Db-Te_dead);
      else  s_Dc=s_Dc-(s_Db+Te_dead);

      if (Incheck<0.0) s_Dn=s_Dn-(s_Db-Te_dead);
      else  s_Dn=s_Dn-(s_Db+Te_dead);
     }
  else if ((s_Db<=Te_dead)&&(Ibcheck<0.0))
    {
      if (Iacheck<0.0) s_Da=s_Da-(s_Db-Te_dead);
      else  s_Da=s_Da-(s_Db-(3.0*Te_dead));

      if (Iccheck<0.0) s_Dc=s_Dc-(s_Db-Te_dead);
      else  s_Dc=s_Dc-(s_Db-(3.0*Te_dead));

      if (Incheck<0) s_Dn=s_Dn-(s_Db-Te_dead);
      else  s_Dn=s_Dn-(s_Db-(3*Te_dead));
```

```
    }
 else if ((s_Dc<=Te_dead)&&(Iccheck>=0.0))
     {
      if (Iacheck<0.0) s_Da=s_Da-(s_Dc-Te_dead);
      else  s_Da=s_Da-(s_Dc+Te_dead);

      if (Ibcheck<0.0) s_Db=s_Db-(s_Dc-Te_dead);
      else  s_Db=s_Db-(s_Dc+Te_dead);

      if (Incheck<0.0) s_Dn=s_Dn-(s_Dc-Te_dead);
      else  s_Dn=s_Dn-(s_Dc+Te_dead);
     }
   else if ((s_Dc<=Te_dead)&&(Iccheck<0.0))
     {
      if (Iacheck<0.0) s_Da=s_Da-(s_Dc-Te_dead);
      else  s_Da=s_Da-(s_Dc-(3.0*Te_dead));

      if (Ibcheck<0.0) s_Db=s_Db-(s_Dc-Te_dead);
      else  s_Db=s_Db-(s_Dc-(3.0*Te_dead));

      if (Incheck<0.0) s_Dn=s_Dn-(s_Dc-Te_dead);
      else  s_Dn=s_Dn-(s_Dc-(3.0*Te_dead));
     }
 else if ((s_Dn<=0.0)&&(Incheck>=0.0))
     {
      if (Iacheck<0.0) s_Da=s_Da-(s_Dn-Te_dead);
      else  s_Da=s_Da-(s_Dn+Te_dead);

      if (Ibcheck<0.0) s_Db=s_Db-(s_Dn-Te_dead);
      else  s_Db=s_Db-(s_Dn+Te_dead);

      if (Iccheck<0.0) s_Dc=s_Dc-(s_Dn-Te_dead);
      else  s_Dc=s_Dc-(s_Dn+Te_dead);
     }
   else if ((s_Dn<=0.0)&&(Incheck<0.0))
     {
      if (Ibcheck<0.0) s_Da=s_Da-(s_Dn-Te_dead);
      else  s_Da=s_Da-(s_Dn-(3.0*Te_dead));

      if (Iccheck<0.0) s_Dc=s_Dc-(s_Dn-Te_dead);
      else  s_Dc=s_Dc-(s_Dn-(3.0*Te_dead));

      if (Iacheck<0.0) s_Da=s_Da-(s_Dn-Te_dead);
      else  s_Da=s_Da-(s_Dn-(3.0*Te_dead));
     }

}
```